A Comparison of Several Constructive Techniques for VLSI Circuit Placement

Z. Yang and S. Areibi
University of Guelph
School of Engineering
Guelph, Ontario
Canada, N1G 2W1
email:zyang@uoguelph.ca, sareibi@uoguelph.ca

July 26, 2002

Abstract

In the past thirty years, VLSI-CAD (Computer-Aided Design of Very Large-Scale Integrated circuits) has been an enabling force behind the exponential growth of the performance and capacity of integrated circuits[1]. The layout of integrated circuits on chips is one of many interrelated complex tasks in VLSI circuit design. In the combinatorial sense, the layout problem is a constrained optimization problem. The most common way of breaking up the layout problem into sub-problems is first to do logic partitioning where a large circuit is divided into a collection of smaller modules according to some criteria, then to perform component placement, and then to determine the approximate course of the wires in a global routing phase after which a detailed-routing phase determines the exact course of the wires in the layout area. A good placement is a key aspect in the design of VLSI circuits, since it has a pronounced affect on the final chip layout. The placement problem is usually subdivided into an initial placement phase and an iterative placement improvement phase. This paper addresses only the initial placement problem for semi-custom designs (i.e designs utilizing standard cell libraries).

Historically, the initial placement of standard cells has been based on one of two major categories of algorithms; specifically, the class of techniques that is constructive in nature (bottom-up approach) and the class that utilizes a top-down partitioning scheme. In this paper we compare several initial placement techniques based on (i) Pair Linking (ii) Cluster Development (iii) Utility Function (iv) Genetic Algorithms (v) Bipartitioning (vi) Quadratic Based Placement. The first three approaches are simple greedy adaptive constructive techniques. Genetic Algorithms and Bipartitioning are assumed to be Meta-Heuristics that are suitable for constructing good initial solutions. The quadratic based placement minimizes a certain quadratic net-length estimation and provides good relative placement with overlaps (a legalization phase follows to produce feasible initial solutions). The performance of these different techniques will be measured on MCNC benchmarks with maximum of 25,000 gates. Both flat and hierarchical approaches will be used to find the effectiveness of these approaches. An iterative improvement approach will follow the initial placement produced by each technique and the robustness will be measured in terms of quality of solutions produced by the initial placement and final placements achieved using the local search heuristic.

References

[1] H. Chang, L. Cooks, and M. Hunt. *Surviving the SOC Revolution.* Kluwer Academic Publishers, London, 1999.