ABSTRACTS OF PAPERS

April 11, 2001

CICC 93

TITLE: A COMBINED EIGENVECTOR TABU SEARCH APPROACH FOR CIRCUIT PARTITIONING

This paper describes the application of the Tabu Search heuristic to guide an efficient interchange algorithm to reduce the number of cut nets for k-partitions that are initially generated by a numerical eigenvector model. Results obtained indicate that the quality of solutions and running time of this method is superior to results obtained from random starting points.

ISCAS 93

TITLE: CIRCUIT PARTITIONING USING A TABU SEARCH APPROACH

Tabu Search is a simple combinatorial optimization strategy that has been applied with great success in applications ranging from graph coloring to scheduling and space planning. This paper describes the application of the Tabu Search heuristic to the circuit partitioning problem. Results obtained indicate that in most cases Tabu Search yields netlist partitions with 10% fewer cut nets than the best netlist partitions obtained by using an interchange method or Simulated Annealing. Moreover, the Tabu Search method is 3 to 20 times faster than Simulated Annealing on tested problems. This paper also describes the benefit of integrating Tabu Search with Simulated Annealing.

TALK: ALASAKA 94

TITLE: A Combined Tabu Search Genetic Algorithm for VLSI Design

The layout of integrated circuits on chips and boards which is part of the VLSI design process is a complex task. Solving this problem using a single processing technique in isolation has proven to be impossible. A solution to the above problem involves integrating stochastic, adaptive and local search approaches as a means to avoid many of the weaknesses inherent in each methodology, while capitalizing on their individual strengths. This paper describes the application of a combined Tabu Search and Genetic Algorithm heuristic to solve the circuit

placement problem. This hybrid system thus attempts to combine the power of decentralized characteristics of Genetic Algorithms with the more localized features of Tabu Search. This results in a very powerful hybrid algorithm to explore and exploit the solution space of the layout problem.

MATH PROGRAMMING 94

TITLE: A Unified Partitioning and Placement Approach Based on Tabu Search Algorithm

VLSI physical design automation is essentially the study of algorithms and data structures related to the physical design process. The objective is to study optimal arrangement of devices on a plane and efficient interconnection schemes between these devices to obtain the desired functionality. A good placement is the major prerequisite for successful routing and effective use of chip area. Depending on the input, the placement algorithms can be classified into two major groups: *constructive placement* and *iterative improvement* methods. In most placement tools, constructive placement algorithms are used for initial placement and are normally followed by one or more (iterative) placement improvement algorithms. The general placement problem is NP-complete and hence, the algorithms used are generally heuristic in nature.

Our Work describes a new constructive placement algorithm based on a partitioning scheme which utilizes Tabu Search to guide the search. Interchange methods usually used for partitioning get stuck at local minima. Tabu Search guides such a heuristic to continue exploration without getting stuck at a local optimum by an absence of improving moves, and without falling back into a local optimum from which it previously emerged. The initial solution to the Tabu Search partitioning algorithm is based on a quadratic model that generates a global initial solution. The optimal continuous value placement will not put modules in appropriate slots. The result will lead to modules overlapping and more or less confined to the center of the region. Our partitioning scheme is used to actually place modules more uniformly on the chip. This is achieved by minimizing the total nets cut and wire length between the rows of the chip. Good initial starting points are very important for the iterative placement procedure. The main advantage is reducing the amount of CPU time for the latter to swap modules between rows and within rows to effectively reduce wire length.

QAP 94

TITLE: Advanced Search Techniques for Circuit Partitioning

Most real world problems especially circuit layout and VLSI design are too complex for any single processing technique to solve in isolation. Stochastic, adaptive and local search approaches have strengths and weaknesses and should be viewed not as competing models but as complimentary ones. This paper describes the application of a combined Tabu Search and Genetic Algorithm

heuristic to guide an efficient interchange algorithm to explore and exploit the solution space of a hypergraph partitioning problem. Results obtained indicate, that the generated solutions and running time of this hybrid are superior to results obtained from a combined eigenvector and node interchange method.

6th ICME

TITLE: An Efficient Solution to Circuit Partitioning Using Tabu Search and Genetic Algorithms

The *modern* philosophy for constructing fast, globally convergent algorithms is to combine a simple globally convergent algorithm with a fast, locally convergent algorithm to form a hybrid. The work in this paper involves exploring and implementing hybrid solutions to the problem of circuit partitioning in VLSI physical design. Results obtained indicate that the generated solutions and running time of a combined Tabu Search and Genetic Algorithm are superior to results obtained from Simulated Annealing and Iterative Improvement methods based on module interchange.

DIMACS 96

TITLE: A GRASP Clustering Technique for Circuit Partitioning

As the complexity of VLSI circuits increases, a hierarchical design approach becomes essential to shorten the design period. Circuit clustering plays a fundamental role in hierarchical designs. Identifying strongly connected components in the netlist can significantly reduce the complexity of the circuit and improve the performance of the design process. The sizes of today's circuits are so large that a top-down partitioning scheme alone is infeasible. Therefore, an effective bottom-up clustering approach is necessary as a preprocessing stage in a hierarchical placement approach. We adapt a basic node interchange for solving the circuit partitioning problem and develop a new clustering technique using a Greedy Randomized Search Procedure (GRASP) that further enhance the performance of these heuristics. Solutions were compared with those obtained by the CPLEX MIP mixed integer programming package. In addition, information obtained from the clustering heuristics were used to improve the performance of the MIP CPLEX mixed integer programming package by reducing the computation time involved by 70% on average.

ISCAS 96

TITLE: AN EFFICIENT CLUSTERING TECHNIQUE FOR CIRCUIT PARTITIONING

As the complexity of VLSI circuits increases, a hierarchical design approach becomes essential to shorten the design period. Circuit clustering plays a fundamental role in hierarchical designs. Identifying strongly connected components in the netlist can significantly reduce the complexity of the circuit and improve

the performance of the design process. A good clustering method should identify groups of cells which will eventually end up together in the final partitioning and placement stages. The sizes of today's circuits are so large that a top-down partitioning scheme alone is infeasible. Therefore, an effective bottom-up clustering approach is necessary as a preprocessing stage in a hierarchical placement approach. In this paper, new clustering techniques that can be used for circuit partitioning and placement are introduced.

IFOR 97

TITLE: A Combined Column Generation Tabu Search Technique for Vehicle Routing and Scheduling

CROSS (**C**ustomisable **RO**outing and **S**cheduling **S**ystem) is a software tool designed to assist the dispatchers in the daily routing and scheduling of bulk products from depots to filling stations. In this paper, the algorithmic "evolution" of *CROSS* is outlined and it is recommended that new algorithmic strategies be investigated. The mandate of the new strategies is to maintain the current functionalities of *CROSS* while improving the quality and robustness of the schedules in the environments in which *CROSS* is either presently or anticipated to be used operationally.

This paper outlines an algorithmic strategy that is currently being developed at SIOP to meet this mandate. The strategy utilizes the same underlying mathematical model that the current *CROSS* is based on. However, it interprets the model in a different way in order to better deal with issues around multi-depot scheduling as well as exploiting recent advances in the field of combinatorial optimization.

CAINE 98

TITLE: An Adaptive Tabu Search Approach For Circuit Partitioning

Advances in the development and refinement of general and advanced search strategies depend in part on identifying the type of adaptation to a specific problem domain that will prove most effective. A worthwhile avenue for research relative to combinatorial algorithm development is the issue of fine-tuning of different parameters that affect the performance of these algorithms. Experimentation indicates that selecting the appropriate parameters that control strategies such

as Tabu Search, Genetic Algorithms and Simulated Annealing has a drastic effect on the quality of the final solution. Many attributes of the solution space can affect the ideal Tabu list size, mutation and crossover rates, and the Annealing schedule in the above mentioned methods. It is important to identify when and how parameters are stable, and devise methods to adjust these parameters depending on problem size and application. This paper introduces a new technique to tune the parameters that control the performance of the Tabu

Search algorithm in a more systematic fashion.

CCECE 98

TITLE: Distributed Advanced Search Techniques for Circuit Partitioning
Parallel and distributed computing systems offer the promise of a quantum leap in the computing power that can be brought to bear on many important problems. The potential for distributed processing exists whenever there are several computers interconnected in some fashion so that a program or procedure running on one machine can transfer control to a procedure running on another. In such an environment we wish to assign optimally the modules of a program to specific processors. The main objective in optimizing is twofold, minimizing the running time of the program and improving the efficiency of the algorithm. Our main task in this work is to develop an environment that allows easy parallelization of the existing sequential algorithms, in which the potential parallelism fits easily into the sequential algorithm. This paper discusses techniques to parallelize advanced search heuristics used to solve the circuit partitioning problem.

CCECE 99

TITLE: GRASP: An Effective Constructive Technique For VLSI Circuit Partitioning
Iterative methods are greedy or local in nature and get easily trapped in local optima. Usually interchange methods fail to converge to optimal solutions unless they initially begin from good starting points. The choice of starting point is a very crucial factor in the performance of the iterative improvement algorithms. GRASP is a random adaptive simple heuristic that intelligently constructs good initial solutions in an efficient manner. Good initial partitions obtained by GRASP allow the iterative improvement method to refine that initial partition quality in a reasonable amount of time, thus reducing the computational time and enhancing the solution quality. Results obtained indicate that on average the cut-size is reduced by 20% and speedups of up to 90% were achieved using the GRASP technique.

ICCAD 99

TITLE: Attractor-Repeller Approach for Global Placement
Traditionally, analytic placement used linear or quadratic wirelength objective functions. Minimizing either formulation attracts cells sharing common signals (nets) together. The result is a placement with a great deal of overlap among the cells. To reduce cell overlap, the methodology iterates between *global optimization* and *repartitioning* of the placement area. In this work, we added

new attractive and repulsive forces to the traditional formulation so that overlap among cells is diminished without repartitioning the placement area. The superiority of our approach stems from the fact that our new formulations are convex and no hard constraints are required. A preliminary version of the new placement method is tested using a set of MCNC *benchmarks* and , on average, the new method achieved 3.96% and 7.6% reduction in wirelength and CPU time compared to TimberWolf v7.0 in hierarchical mode.

RAISC 99

TITLE: The Effect of Clustering and Local Search on Genetic Algorithms

Genetic Algorithms **(GA's)** are a class of optimization algorithms that seek improved performance by sampling areas of the parameter space that have a high probability for leading to good solutions. There are many characteristics of Genetic Algorithms which qualify them to be a robust based search procedure. Still there are drawbacks. Genetic Algorithms are not well suited to perform finely tuned search. In this paper we show the advantage of combining local search and clustering techniques with Genetic Algorithms to solve the circuit partitioning problem. Results obtained indicate that this approach achieves on average 35 % improvement in solution quality and 20 % improvement in run time over a conventional GA technique.

CCECE 2000

TITLE: Simple Yet Effective Techniques to Improve Flat Multiway Circuit Partitioning

Partitioning plays an important role in solving large, complicated design problems. For large benchmarks iterative improvement methods based on the Conventional Kernighan and Lin Heuristic produce inferior results. These algorithms suffer from a propensity to freeze the movement of large cells that would immediately violate the balance constraint. To enhance the stability and quality of partitioning results a novel algorithm intensifies the capability of escaping from local optimal by first releasing the size constraint temporarily and enforcing it at the end of a run and controlling the migration direction and secondly by adding a dynamic hill climbing capability to avoid the possibility of getting trapped in a local minima. These simple heuristic techniques reduce the total cut on average by 30% and runtime by at least 70-90%.

CSCC 2000

TITLE: Efficient Hybrid Search Techniques For Circuit Partitioning

Recently, four search approaches have emerged for handling complex combinatorial optimization problems: *Simulated Annealing*, *Genetic Algorithms*, *Tabu*

Search and *Greedy Randomized Search Procedure (GRASP)*. Based on simple ideas, these heuristics have been extremely efficient in finding near-optimal or optimal solutions for many types of difficult problems. In this paper we apply these approaches to the circuit partitioning problem highlighting their strengths and weaknesses. Two hybrid search techniques for the partitioning problem are developed by using GRASP and a Genetic Algorithm to generate good initial partitions. Tabu Search is used to refine the solution quality and reduce the overall computational time of the simpler stand-alone search techniques. Very promising results show the advantages of combining the strengths of these newer search methods.

WOMA 2000

TITLE: An Integrated Genetic Algorithm With Dynamic Hill Climbing for VLSI Circuit Partitioning

Genetic Algorithms **(GA's)** are a class of optimization algorithms that seek improved performance by sampling areas of the solution space that have a high probability for leading to good solutions. In this paper we show the advantage of combining a dynamic hill climbing local search heuristic and the relaxation of size constraint with Genetic Algorithms to solve the circuit partitioning problem. The combined implementation enhances the stability and quality of partitioning results by intensifying the capability of escaping local optimal. Results obtained indicate that this approach achieves on average 40%-60% improvement in solution quality at the expense of a slight increase in computation time over a conventional GA technique.

Smart Systems 2001

TITLE: A Smart Reconfigurable Visual System for the Blind

"Way-finding" refers to the techniques used by people who are blind or visually impaired as they move from place to place independently. People who are blind, deaf, or have other disabilities could greatly benefit from computers and the Internet. In response, we have investigated a wearable stereo-vision system and a prototype system has been developed. Preliminary investigations have proven the viability of this device for navigation through simple hallway structures. The prototype is inexpensive and consists of two USB cameras, a "virtual touch" feedback system and a wearable computer in the form of an inexpensive laptop. Depth measures were computed using a pixel-to-pixel correspondence method making use of an epipolar geometry constraint. We also investigate the usage of a Reconfigurable Computing platform that replaces the laptop as a wearable computer system. Since image processing algorithms are time consuming we suggest to map portions of the pixel-to-pixel algorithm to a platform where they can be executed in real time, hence improving the performance of the overall system.

CATA 2001

TITLE: A New Model for Macrocell Partitioning
This paper investigates a novel approach to the macrocell partitioning problem. Macrocell partitioning is a particularly demanding instance of the general partitioning problem, characterised by highly connected, variable-sized cells. First, we present a formulation of the macrocell partitioning problem as a mixed-integer program. Then we propose a new uniform-cell model for a macrocell circuit which models each macrocell as a clique of equal sized cells. The weights within the clique are chosen such that common partitioning schemes do not break a clique amongst partitions. Initial results using the new model are promising.

CCECE 2001

TITLE: An Efficient Rectilinear Steiner Tree Algorithm for VLSI Global Routing
As we move to deep sub-micron designs below 0.18 microns, the delay of a circuit, as well as power dissipation and area, is dominated by interconnections between logical elements (i.e. transistors). The focus of this paper is on the global routing problem. Both global and channel routing are NP-hard; therefore, all existing solution methodologies are heuristics. The main aim is to develop an efficient K Rectilinear Steiner Trees (K-RST) algorithm. A k-RST routine is developed to generate a set of rectilinear Steiner trees for each net. The K-RST uses local tree segment transformations to ensure that there is no duplication of routing trees for a net. The shortest tree for a net is in general 11% shorter than that of the minimal spanning tree, which leads to area savings.

ERSA 2001

TITLE: A Utility-Based Iterative Improvement Heuristic for Standard-Cell Placement
This paper investigates a novel approach to iterative improvement in the standard-cell placement problem. The method is based on a utility selection criterion, which identifies poorly placed cells based on their closeness to a measure of ideal placement. Experimental results show execution time can be significantly reduced over a simple greedy placement algorithm.

ICAI 2001

TITLE: A Comparison of Genetic/Memetic Algorithms and Other Heuristic Search Techniques
Iterative improvement techniques based on module interchange are the most robust, simple and successful heuristics in solving the partitioning and placement

problems. Interchange methods fail to converge to "optimal" or "near optimal" solutions unless they initially begin from "good" initial starting points. In this paper we compare the performance of several constuctive based techniques for the circuit partitioning problem.

GECCO 2001

TITLE: Memetic Algorithms for VLSI Physical Design: Implementation Issues

Incorporation of local improvement operators into the recombination step of a Genetic Algorithm is essential if a competitive Genetic Algorithm is desired. Memetic Algorithms (MAs) are Evolutionary Algorithms (EAs) that apply a separate local search process to refine individuals (i.e improve their fitness by hill-climbing). Under different contexts and situations, MAs are also know as hybrid EAs, genetic local searchers. In this paper we describe our experience on using different types of Memetic Algorithms on the VLSI circuit partitioning problem. Results obtained indicate that Memetic Algorithms based on local search, clustering and good initial solutions based on GRASP improve solution quality by 80% for the VLSI circuit partitioning problem.

SCI 2001

TITLE: Iterative Improvement Heuristics for the Standard Cell Placement: A Comparison

As we move to deep sub-micron designs below 0.18 microns, the delay of a circuit, as well as power dissipation and area, is dominated by interconnections between logical elements (i.e. transistors)[**?**]. This paper introduces and compares several iterative heuristic search techniques for the Standard Cell VLSI Placement problem.

SCI 2001

TITLE: Area and Power Minimization of CMOS Combinational Circuits Using a Modified Simulated Annealing Technique

Chip area, power consumption and signal delay are critical and conflicting criteria for optimal design of high performance digital VLSI circuits. In this paper, a modified simulated annealing algorithm is proposed to minimize the area and power of CMOS combination circuits with given delay constraint.

ICECS 2001

TITLE: Exploration and Exploitation in Genetic Algorithms For Graph Partitioning

Circuit partitioning is an application of hypergraph partitioning, which, also, has application in areas such as data mining and efficient storage of large data bases on disks. In this paper, the exploration and exploitation capabilities of a Genetic Algorithm are combined with a local interchange method to form a hybrid optimization technique to provide a good solution to the NP-hard netlist partitioning problem.

FIE 2001

TITLE: A First Course in Digital Design Using VHDL and Programmable Logic

Present industry practice has created a high demand for systems designers with knowledge and experience in using programmable logic in the form of CPLDs and FPGAs in addition to hardware description languages. Many universities offer this type of training in advanced digital engineering courses. This paper describes our experience in integrating VHDL and programmable logic devices based on Xilinx Foundation tools and Altera into a first course in logic design. In the main, student reaction to the course was positive. The course seems to have the right blend of being current (using VHDL and FPGAs) and being hands-on (using bread-boarding). We conclude by stating that in our experience, modeling using VHDL and mapping designs to FPGAs can be effectively integrated into a first course in logic design.

13th ICME 2001

TITLE: Recursive and Flat Partioning for VLSI Circuit Design

As we move to deep sub-micron designs below 0.18 microns, the delay of a circuit, as well as power dissipation and area, is dominated by interconnections between logical elements (i.e. transistors). The focus of this paper is on recursive partitioning problem.