Statement of Research Activity

Dr. Shawki Areibi **PhD Computer Engineering**

My research interests are focused in the areas of **VLSI CAD**, **Combinatorial Optimization**, **Advanced Heuristic Search Techniques** and **Embedded Systems** (Hardware/Software Co-design) and **Reconfigurable Architectures**.

VLSI Physical Design Automation

This research activity addresses the problem of VLSI circuit layout. The research deals with the algorithms that are used inside VLSI design automation tools, also called computer-aided design (CAD) tools. VLSI stands for Very Large Scale Integration, which refers to those integrated circuits that contain more than 1 million transistors. The circuits designed may be general-purpose such as microprocessors and memories or application-specific integrated circuits (ASICs) which are designed for a narrow range of applications. Designing such a circuit is a difficult task. A first requirement is, of course, that a given specification is realized. Besides this, there are different entities that one would like to optimize. These entities can often be optimized simultaneously. The most important entities are: Area Minimization of the chip to increase the yield, Speed, Power dissipation, Design time and Testability. I have made significant contributions to this topic of research especially to performance driven layout. I proposed novel techniques to solve the circuit partitioning and placement problems efficiently which are published in international journals and conferences. A Masters student co-supervised by Dr. A. Vannelli was able to develop new clustering based placement heuristics and utility based iterative placement techniques that are comparable to those developed by industry. Currently collaboration with *Sapphire Design Automation* in San Jose are carried out to develop a state of the art Global Router for their placer.

Reconfigurable Architectures for Hardware Accelerators

Reconfigurable Computing Systems are computers based on hardware, most of which can be arbitrarily defined to suit the needs of the particular problem to be solved. The goal of configurable computing is to achieve most of the performance of custom architectures while retaining most of the flexibility of general purpose computing. The main objective of this research activity is to design state of the art hardware accelerators to speedup the performance of combinatorial optimization heuristics and control algorithms based on Tabu Search, Genetic Algorithms, Neural Networks and Fuzzy Logic. Currently I am working on several advanced search heuristics for solving the VLSI circuit layout problem which require custom design hardware accelerators to obtain solutions in minimum CPU time. Some of the problems that can benefit from these advanced search techniques are

graph partitioning, facility layout, global and detailed routing. The main idea is to divide the algorithm into sequentially executed stages. This process of "configure and execute" is repeated until the algorithm has completed its task. A Masters student is currently working on a reconfigurable computing platform to design a real time fuzzy controller for a robot.

Algorithms and Search Heuristics for Optimization

Combinatorial optimization study problems, which are characterized by a finite number of feasible solutions, abound in everyday life, particularly in engineering design. An important and widespread area of applications concerns the efficient use of scarce resources to increase productivity. Typical engineering design problems relate to set covering, bin packing, knapsack packing, quadratic assignment, minimum spanning tree determination, vehicle routing and scheduling, facility location and so on. Engineering optimization and advanced search heuristics in the form of Tabu Search, Simulated Annealing, Genetic Algorithms and GRASP are indispensable working tools for industrial engineers and designers, as well as systems analysts, operations researchers, and management scientists working in manufacturing and related industries.I have proposed several novel techniques to reduce the complexity of problems via clustering and partitioning and also hybrid approaches that were very effective in solving combinatorial optimization problems in general and circuit layout in particular. Results of this research have been published and presented in several IEEE International Conferences on CAD, Operations Research and VLSI Design. A Masters student joining in the Winter 2001 will be studying the possibility of combining exact mathematical techniques with advanced search heuristics to solve several problems in VLSI circuit layout.

Parallel and Distributed Architectures

Parallel and distributed computing systems offer the promise of a quantum leap in the computing power that can be brought to bear on many important problems. The potential for distributed processing exists whenever there are several computers interconnected in some fashion so that a program or procedure running on one machine can transfer control to a procedure running on another. The main objective in optimizing is twofold, minimizing the running time of the program and improving the efficiency of the algorithm. In this area I have dealt with developing an environment that allows easy parallelization of existing sequential algorithms and also in developing custom hardware accelerators dedicated for distributed simulations. Simulations of complex Discrete Event Systems are usually exceedingly slow and are notorious consumers of CPU cycles. It is therefore becoming an increasingly important research goal to speed up simulations by exploiting concurrency inherent in them. The main goals of this research are to investigate the feasibility of performing distributed discrete event simulations based on the Time Warp Mechanism.

Hardware/Software Co-Designs for Embedded Systems

Embedded controllers for reactive real-time applications are implemented as mixed software-hardware systems. These controllers utilize Micro-processors, Micro-controllers and Digital Signal Processors but are neither used nor perceived as computer. Generally, software is used for features and flexibility, while hardware is used for performance. Design of embedded systems can be subject to many different types of constraints, including timing, size, weight, power consumption, reliability, and cost. Current methods for designing embedded systems require to specify and design hardware and software separately. The main research contributions to this area is developing a methodology for specification, automatic synthesis, and validation of this sub-class of embedded systems. Design is done in a unified framework, with a unified hardware-software representation, so as to prejudice neither hardware nor software implementation. Previous techniques developed for VLSI Circuit Partitioning are modified to accommodate the difficulty of combining components that exhibit different characteristics.

Multi Agent Systems for Optimization/Manufacturing

Intelligent software agents are a unique generation of information society tools that independently perform various tasks on behalf of human user(s) or other software agents. The new possibility of information society requires the Development of new more intelligent methods, tools and theories for modelling/engineering of agent-based systems and technologies. Global competition and rapidly changing customer requirements are forcing major changes in the production sytles and configuration of manufacturing organizations. Agent technology provides a natural way to overcome such problems, and to design and implement distributed intelligent manufacturing environments. Our research focuses on the idea of integration from the perspective of rapidly deployable distributed systems as applied to distributed optimization problems and manufacturing systems.