(When) Will FPGAs Kill ASICs?

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FPGAs vs. ASICs

- Cost – the real story.
- Time to market
- Why choose ASICs?
- Where are FPGAs going?
Unit Cost Analysis

Total cost

ASIC Costs
Start higher, but slope is flatter

For each technology advance, crossover volume moves higher

Volume K units
Cost: The exploding ASIC NRE

Source: Dataquest
Time to market is critical

Potential profit if you come early to the market

Long time to market is a cost

What you get if you design with an ASIC and come late to the market

Missing the market window will wipe out all savings from development and production

Revenue

Start of market window

End of market

Time

FPGA

ASIC
COST: System Reconfigurability

Without reconfigurability (with ASICs)

Extend the market window with reconfigurability (with FPGAs)

Lack of reconfigurability is a huge opportunity cost of ASICs.

FPGAs offer flexible life cycle management.
Breakeven Cost: Just the facts

- Total cost
- ASIC
- Time-to-market
- Re-spins & Inventory
- Unit cost
- Volume K units
Time To Market: Design Cycle

ASIC
Spec | Design & verification | Silicon | System Integration | Production | First Ship

FPGA
Spec | Design and verification | System Integration | Production | First Ship

• ASIC Methodology is very unforgiving
• FPGA flexibility allows late design changes
Designing with ASICs

Timing Closure is a very serious problem in DSM

Verification

DSM Effects

Process issues
Designing with FPGAs

Verification is much simpler

Timing Closure is a much simpler problem in FPGAs

Super fast compile times
~1M gates in < 1hr
Why do people design ASICs?

- Cost/Volume
- Performance
- Density
- IP Libraries
Volume requirement for ASICs

- Cost
- Density
- Performance
- IP Libraries

>50% of market is available today for FPGAs

Source: IMS 2000
Gate count requirement for ASICs

- Cost
- Density
- Performance
- IP Libraries

FPGAs can address very large part of the ASIC market today

Source: IMS 2000
Performance requirement for ASICs

- Cost
- Density
- Performance
- IP Libraries

![Pie chart showing performance requirements for ASICs]

- <100Mhz: 53.9%
- 100-200Mhz: 38.5%
- >200Mhz: 10.8%

FPGAs can address very large part of the ASIC market today

Source: IMS 2000
5 Years ago FPGAs were only gates and routing ~25000 gates

Today, there are several system-level features. ~10,000,000 gates

The trend to add more IP in FPGAs continues
The Question is …

- The question is not if FPGAs will kill ASICs
  - Everyone understands the advantages of programmability

- The real question is “How can I get programmability in my system?”

- More IP on an FPGA or Programmability on an ASIC?
## What is the future? You decide…

<table>
<thead>
<tr>
<th></th>
<th>More IP on FPGA</th>
<th>More Prog. On ASIC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Time-to-market</strong></td>
<td>Verification remains simple</td>
<td>Verification remains a problem</td>
</tr>
<tr>
<td></td>
<td>Timing closure is easier</td>
<td>Timing closure remains an issue</td>
</tr>
<tr>
<td><strong>Cost</strong></td>
<td>NRE is non-existent</td>
<td>NRE not reduced</td>
</tr>
<tr>
<td></td>
<td>Extensive reconfigurability</td>
<td>Very limited reconfigurability</td>
</tr>
<tr>
<td><strong>Design methodology/Software</strong></td>
<td>Simple methodology &lt;br&gt; Ease of use &lt;br&gt; Extremely fast SW runtimes</td>
<td>Still a complex methodology &lt;br&gt; Ease of use is still lacking</td>
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</tbody>
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