ENG-2410 Assignment #4

School of Engineering, University of Guelph
Fall 2025

Start Date: Week #4, Due Date: Week #5 (Friday, 5:00 PM) in Dropbox

Answer all questions.

1. **Design** a combinational circuit that detects an error in the representation of a decimal digit in BCD. In other words, obtain a logic diagram whose output is equal to **1** when the inputs contain any one of the six unused bit combinations in the BCD code.
   (a) **Derive** the truth table.
   (b) **Use K-Maps** to minimize the logic.
   (c) **Derive** the Boolean expression.
   (d) **Draw** the logic diagram.
2. A minority function is generated in a combinational circuit when the output is equal to **1** if the input variables have more **0's** than **1's**. The output is **0** otherwise. **Design** a 3-input minority function. **Derive** the truth table. **Derive** the Boolean Expression. **Use K-Maps** to minimize the Boolean Equation. **Draw** the logic diagram.
3. **Design** a combinational circuit that accepts a 2-bit number and generates a 4-bit binary number output equal to the square of the input number.
4. A low-voltage lighting system is to use a binary logic control for a particular light. This light lies at the intersection point of a T-shaped hallway. There is a switch for this light at each of the three end-points of the T. These switches have binary outputs 0 and 1 depending on their position and are named X_1, X_2 and X_3. The light is controlled by an amplifier driving a thyristor. When Z, the input to the amplifier, is 1, the light is ON and when Z is 0, the light is OFF. You are to **find the function** $Z = F(X_1, X_2, X_3)$ so that if any one of the switches is changed, the value of Z changes turning the light ON or OFF.
5. This question is related to Universal Gates:
   (a) **Why** is the NAND gate referred to as a Universal Gate?
   (b) **Prove** that a NAND gate is Universal.
   (c) **Implement** the following Boolean Function $F = A(\bar{B} + \bar{C}) + E(\bar{D})$ using AND, OR, NOT gates.
   (d) **Redesign** the circuit above using **NAND** gates only.

6. **Draw** the NAND logic diagram for each of the following expressions, using a multiple-level NAND circuit:

   (a) $W(X + Y + Z) + XYZ$

   (b) $(\bar{A}B + C\bar{D})E + B\bar{D}(A + B)$

Deliverable

- **Name your file** as follows: ENG2410_F25_Assignment4_LastNameFirstName.pdf
- **Write** your name, the course # and Term # on the first page of your submission (i.e solution).
- **Submit** a single PDF file of your solutions.
- **Upload** your PDF file in the Course Link dropbox.
- **Late** submissions are not accepted.
- Your solution of the assignment will **not be accepted** via email.
- To **receive 100% of the mark** you should attempt all questions.
- Solutions to the assignment will be posted at 5:30 PM on Fridays.
- If you have any questions related to the assignment, please **contact your Teaching Assistant** responsible for your Tutorial Section.
- Failing to follow the instructions above will lead to a ZERO grade!!