Nexys3 BSB Support Files for PLB-based Designs

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Overview

This package will integrate board support for the Nexys3 Spartan-6 FPGA Development Board into Xilinx EDK tools. It includes board definition files for creating PLB-based MicroBlaze embedded designs in the Base System Builder (BSB). It also includes cores for custom peripherals such as the Digilent Usb-Epp interface, the 16MB Quad SPI Flash Memory and the 4-digit Seven-Segment Interface. With these files the BSB can be used to create Platform Studio projects initialized with cores that are properly configured to control the on-board peripherals. The currently supported cores are outlined in Table 1.

TABLE 1. BSB SUPPORTED PERIPHERALS

Peripheral	Peripheral name in BSB	Core name(s)	Notes
User Reset			BTNS is automatically assigned as the system reset input
16 MB PSRAM	Micron_RAM	xps_mch_emc	Any combination of these memories can be selected; a memory bus multiplexer
16-MB Parallel PCM	Numonyx_PCM	xps_mch_emc	resolves the shared buses; Digilent_quad_spi_if is a custom core;
16MB SPI PCM in Quad mode	Digilent_quad_spi _if	quad_spi_if	supports 1X, 2X and 4X modes
8 User Switches	Switches_8Bit	xps_gpio	
4 User Push Buttons	Push_Buttons_4B it	xps_gpio	BTNS (the center button) is automatically assigned as the system reset input
8 LED outputs	LEDs_8Bit	xps_gpio	
UART	RS232_Uart_1	xps_uartlite/xp s_uart16550	
PS2 Keyboard or Mouse interface through USB	PS2_Mouse_Key board	xps_ps2	BSB does not connect automatically the interrupt outputs. It is recommended that after the BSB is generated to connect manually the Interrupt outputs to an interrupt controller
10/100/1000 Mbps Ethernet PHY	Soft_TEMAC	xps_II_temac	Requires a license, otherwise will stop functioning on the board after a period of time
10/100 Mbps Ethernet PHY	Ethernet_MAC	xps_ethernetlit e	Currently only functions properly when used at 10 Mbps, see below; exclusive to Soft TEMAC
Digilent Usb-Epp interface	Digilent_Usb_Epp	d_usb_epp_ds tm	Custom core; DSTM transfer mode support in future release
Seven-Segment Decoder	Ssg_Decoder_0	Ssg_decoder	Supports individual digit blanking and blinking, autoblank, variable refresh rate and blink rate and individual segment data



For additional information on using these cores, please refer to their PDF datasheets

Using the BSB Support Files

Use the BSB Support Files for PLB as a Project Peripheral Repository Search Path such as in the example below:

- 1. Start Platform Studio and create a new project in Base System Builder. Choose PLB system in the "Create New XPS Project Using BSB Wizard" window.
- 2. Click on the "Browse" button beside the "Set Project Peripheral Repository Search Path" box and browse to the path containing the .\lib subfolder from the BSB Support Files folder, then press OK. The BSB window should look like in the figure below:

Create New XPS Project Using BSB Wizard					
New Project Project File D:\Digilent\Projects\Wexys3\Wexys3_PLB_BSB\system.xmp Browse					
Select an Interconnect Type					
AXI system AXI is an interface standard recently adopted by Xilinx as the standard interface used for all current and future versions of Xilinx IP and tool flows. Details on AXI can be found in the AXI Reference Guide on xilinx.com.					
PLB System PLB is the legacy bus standard used by Xilinx that supports current FPGA families, including Spartan6 and Virtex6. PLB IP will not support newer FPGA families, so is not recommend for new designs that may migrate to future FPGA families. Details on PLB can be found in the PLBv46 Interface Simplifications document on xilinx.com.					
Select Existing .bsb Settings File(saved from previous session)					
Set Project Peripheral Repository Search Path					
:\Digilent\Board_Support_Files_EDK\Wexys3_BSB_Support_v_2_3\Wexys3_PLB_BSB_Support\\ib Browse					
Help OK Cancel					

Figure 1. BSB window with specifying the Peripheral Repository Search Path

Click OK. You should now be able to select the Digilent Nexys3 as your development board further in the Board Selection window.

Using Interrupt for the Digilent Usb-Epp interface

EPP requests for the USB-EPP interface come from the USB port. If there is no answer in 100mS, the PC application will signal a timeout. Therefore, it is recommended that Epp requests are handled with an interrupt service routine instead of continuously polling the interface status. In order to use interrupt service routines, the interrupt request signal for the Digilent USB-EPP has to be connected to either an interrupt controller or the Microblaze processor interrupt input.

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This can be done in BSB in the "Peripheral Configuration" window. Click on the "Digilent_Usb_Epp" peripheral and select "Use Interrupt" like is shown in Figure 2 below.

📀 Base System Builder					? X
Welcome Board	System	Processor	Peripheral	Cache	Summary
Peripheral Configuration To add a peripheral, drag it from the "Available Peripherals	erals" to the proc	essor peripheral list. To	o change a core parameter,	click on the periphe	ral.
Peripheral Names		Processor 1 (MicroBla	aze) Peripherals		Select All
 IO Devices ETHERNET mem_bus_mux_0 Internal Peripherals Imb_bram_if_cntlr xps_bram_if_cntlr xps_timebase_wdt xps_timer 		Core DIP_Switches_8Bit Core: xps_gpio Digilent_QuadSPI Core: quad_spp Digilent_SevSeg_D Core: ssg_dec Digilent_Usb_Epp Core Use Interrupt Ethernet_Lite Core: xps_ethe LEDs_8Bits Core: xps_gpio	is _Cntlr vi_if Disp oder ernetlite	Parameter	lstm

Figure 2. Connecting the interrupt output for the Digilent_Usb_Epp interface in Base System Builder.

In this case, BSB will automatically add an interrupt controller to the system and connect the Usb_Epp interface interrupt output to the interrupt controller. The interrupt signal priority depends on what other interrupt signals are used in the system.

It is also recommended to use interrupts for the PS2-HID interface if using a mouse, due to the increased data rate of the mouse. BSB does support auto-connect for the PS2 interrupt signals, but these signals can be manually connected after the Base System is generated by using the System Assembly view's Ports tab.

Notes about the mem_bus_mux core:

In the "Peripheral Configuration" window, the "Available Peripherals" (left-side) pane contains a peripheral names mem_bus_mux_0, with the core named mem_bus_mux. This core is used to split and multiplex the address and data buses for the three memories present in the system. The core is automatically added to the Base System and **does not have to be added by the user.** Adding the core to the system does not affect the system functionality.

Using the Parallel Flash:

In the "Cache Configuration" window, both the Micron_RAM (PSRAM) and the Numonyx_PCM (Flash) memory appear as cacheable. Using caches is recommended because of the faster code execution and data read/write.



However, writing directly into the FLASH memory is not yet supported. If using caches, avoid selecting the Numonyx_PCM for data cache memory.

The standard parallel Flash device on the Nexys3 is a 16Mbyte Micron Parallel PCM Flash. If the board has a larger Flash device, the user must increase the Flash Memory address space in System Assembly View after the Base System is generated. To do this:

- 1. In System Assembly View, click on the Adresses Tab and change the size of the Numonyx_PCM memory to the appropriate size. See Figure 3 below.
- 2. Click on the "Generate Adresses" button

□₽×	B X B Bus Interfaces Ports Addresses									
	Instar	nce	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name	Lock	
	⊖-microblaze 0's Address Map									
		- dlmb_cntlr	C_BASEADDR	0x00000000	0x00003FFF	16K	SLMB	dlmb		
		- ilmb_cntlr	C_BASEADDR	0x00000000	0x00003FFF	16K	SLMB	ilmb		
md		- Ethernetlite	C_BASEADDR	0x81000000	0x8100FFFF	64K	SPLB	mb_plb		
ntime.op		Switches_8Bit	C_BASEADDR	0x81400000	0x81405FFF	64K	SPLB	mb_plb		
		- Push_Buttons_4Bit	C_BASEADDR	0x81420000	0x8142FFF	64K	SPLB	mb_plb		
		LEDs_8Bit	C_BASEADDR	0x81440000	0x8144FFFF	64K	SPLB	mb_plb		
		xps_intc_0	C_BASEADDR	0x81800000	0x8180FFFF	64K	SPLB	mb_plb		
		RS232_Uart_1	C_BASEADDR	0x84000000	0x8400FFFF	64K	SPLB	mb_plb		
		mdm_0	C_BASEADDR	0x84400000	0x8440FFFF	64N	SPLB	mb_plb		
		- Micron_RAM	C_MEM0_BASE	0x85000000	0x85FFFFFF	16M	SPLB	mb_plb		
		PS2_Mouse_Keyboard	C_BASEADDR	0x86A00000	0x86A0FFFF	64K	SPLB	mb_plb		
		- Numonyx_PCM	C_MEM0_BASE	0x87000000	0x87FFFFFF	16M	SPLB	mb_plb		
		Ssg_Decoder_0	C_BASEADDR	0xC6A00000	0xC6A0FFFF	64K	SPLB	mb_plb		
		- Digilent_Usb_Epp	C_BASEADDR	0xCBC00000	0xCBC0FFFF	64K	SPLB	mb_plb		
		- Digilent_quad_spi_if	C_BASEADDR	0xCD600000	0xCD60FFFF	64K	SPLB	mb_plb		

Figure 3. Changing the size of the Numonyx_PCM Flash memory

After increasing the address space size, it is necessary to regenerate the addresses. This is due to the fact that each base address has to start from a value for which the least significant number of bits that form the address space must be 0. For example, if the Numonyx_PCM size increases to 64MB, the the current base address, 0x87000000 is incorrect, because only the least significant 24 bits are 0. A correct address would be 0x8C000000, where the least significant 26 bits are 0.



Notes about using the xps_ethernetlite core:

Currently, the Nexys3 onboard SMSC PHY functions with the Ethernetlite core only in 10Mbps mode and only if global buffers are enabled for the RXCLK and TXCLK inputs.

For Spartan6 devices, this parameter is unsupported by Platform Studio. However, enabling the global buffers can be done by modifying the .mhs file in Platform Studio:

a. In the Project pane, double-click the sytem.msh file, as Figure 4 below shows:



Figure 4. Opening the .mhs file in Platform Studio

b. After the .mhs file is opened, scroll down to the "BEGIN xps_ethernetlite" line. Insert after this line the following parameter value: "PARAMETER C_INCLUDE_GLOBAL_BUFFERS = 1", as Figure 5 below shows:



Figure 5. Enabling global buffers for Ethernet_Lite in the .mhs file

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c. Save the system.mhs file (from the menu choos File->Save). Platform Studio will ask about reloading the project, because the .mhs file has been changed. Answer either "Reload" or "Always Reload".

The PHY can be set in 10MBps mode by clearing the Speed Select bit (Bit 13) in the PHY's Basic Control Register. For details, please refer to the SMSC LAN8710A/LAN8710Ai datasheet.

Note that the Peripheral Test application generated by SDK by default sets the PHY speed to 100Mbps. Look to the demo applications on the Digilent website for an example how to set the Ethernet PHY to 10MBps mode.

Using the xps_II_temac (Soft_TEMAC) core

The Soft_TEMAC core requires a license to run, although EDK offers an evaluation license which allows the core to function on the board for a period of time. The core allows operation at 100Mbps with the SMSC PHY.

Due to the size of the Spartan-6 FGPA device on the Nexys3 board, using the xps_II_temac core core may not allow all of the selected peripherals in the system to fit. It is recommended that peripherals not used by the application be deselected.