

Nexys 3 board tutorial

(Decoder, ISE 13.2)

Jim Duckworth, August 2011, WPI.

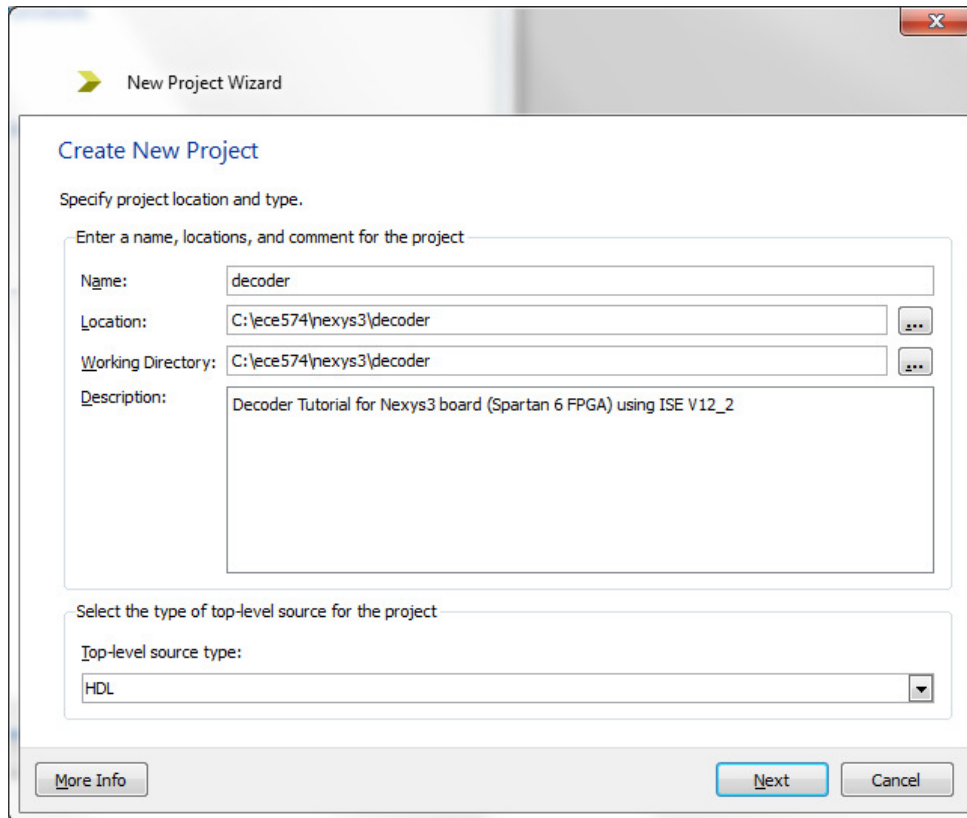
Note: you will need the Xilinx ISE Webpack installed on your computer (or you can use the department systems).

[Note you can also review Xilinx Tutorials, for example, under Design Resources: ISE Design Suite Tutorials, and ISE Design Suite Logic Edition - Quick Tour]

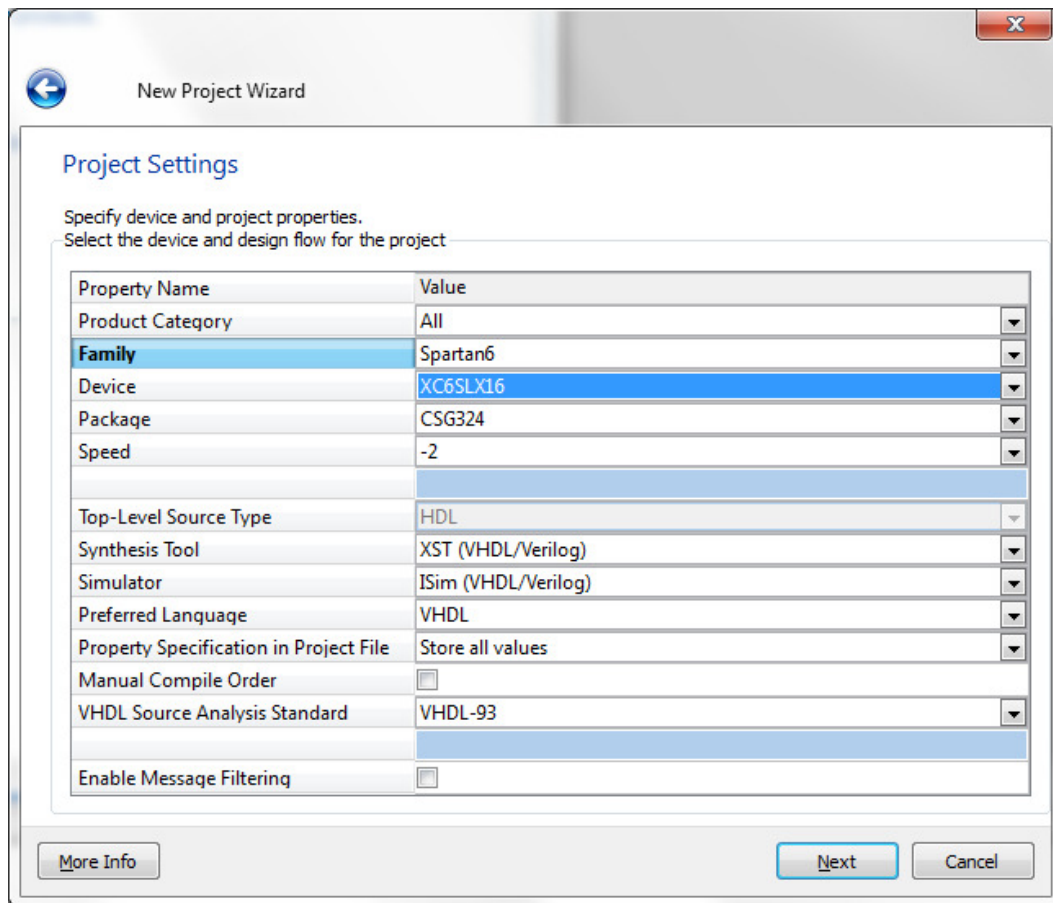
Start Xilinx ISE Design Suite,

Select **File => New Project** or click on **New Project**

and enter "decoder" for the project name (select an appropriate location):



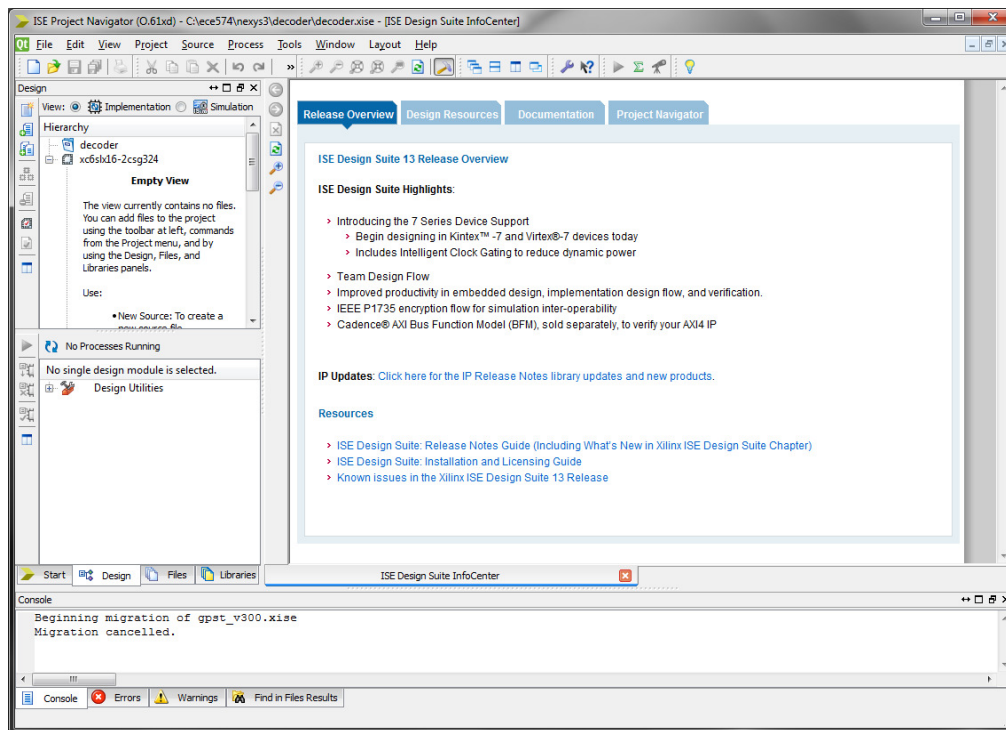
Click **Next** and carefully select the family, device, package, etc to match the FPGA on the Nexys 3 board (also select ISim for the simulator):



The image shows the 'New Project Wizard' dialog box, specifically the 'Project Settings' step. The title bar says 'New Project Wizard' with a back arrow icon on the left and a close 'X' icon on the right. Below the title bar, the text 'Project Settings' is displayed in blue. Underneath, it says 'Specify device and project properties. Select the device and design flow for the project'. The main area contains a table with two columns: 'Property Name' and 'Value'. The 'Family' row is highlighted in blue, and the 'Device' row is also highlighted in blue. The 'Value' column for 'Device' shows 'XC6SLX16'. Other properties include 'Product Category' (All), 'Package' (CSG324), 'Speed' (-2), 'Top-Level Source Type' (HDL), 'Synthesis Tool' (XST (VHDL/Verilog)), 'Simulator' (ISim (VHDL/Verilog)), 'Preferred Language' (VHDL), 'Property Specification in Project File' (Store all values), 'Manual Compile Order' (unchecked), 'VHDL Source Analysis Standard' (VHDL-93), and 'Enable Message Filtering' (unchecked). At the bottom, there are three buttons: 'More Info', 'Next', and 'Cancel'.

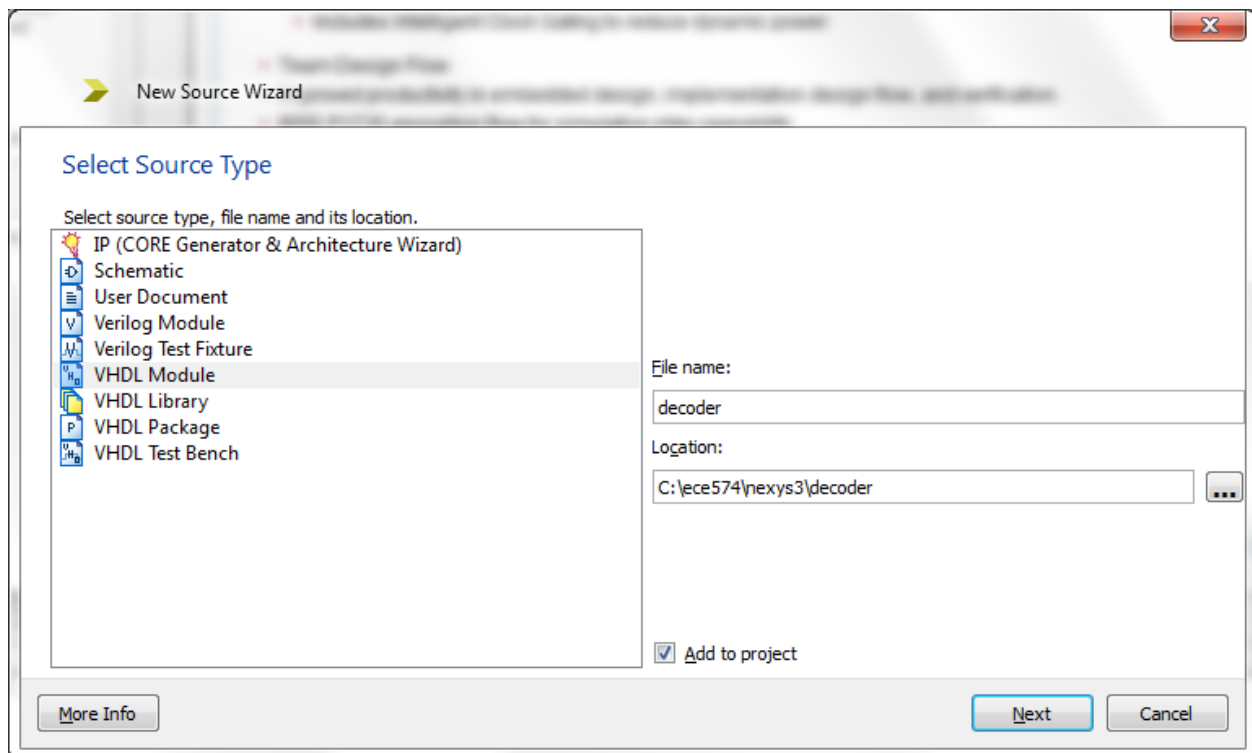
Property Name	Value
Product Category	All
Family	Spartan6
Device	XC6SLX16
Package	CSG324
Speed	-2
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	VHDL
Property Specification in Project File	Store all values
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>

Click **Next**, and then click **Finish**

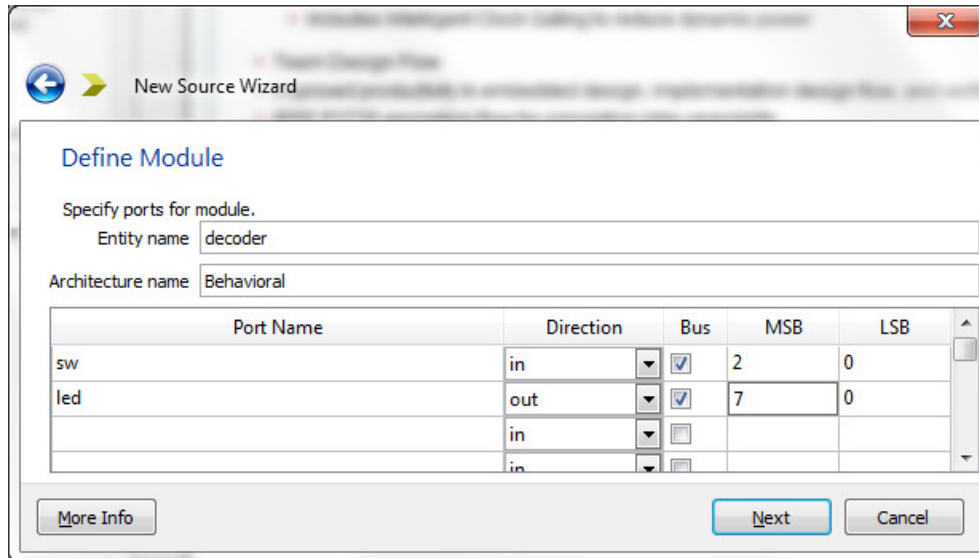


Click on **New Source** (top left icon in the Design window), or menu option **Project => New Source**.

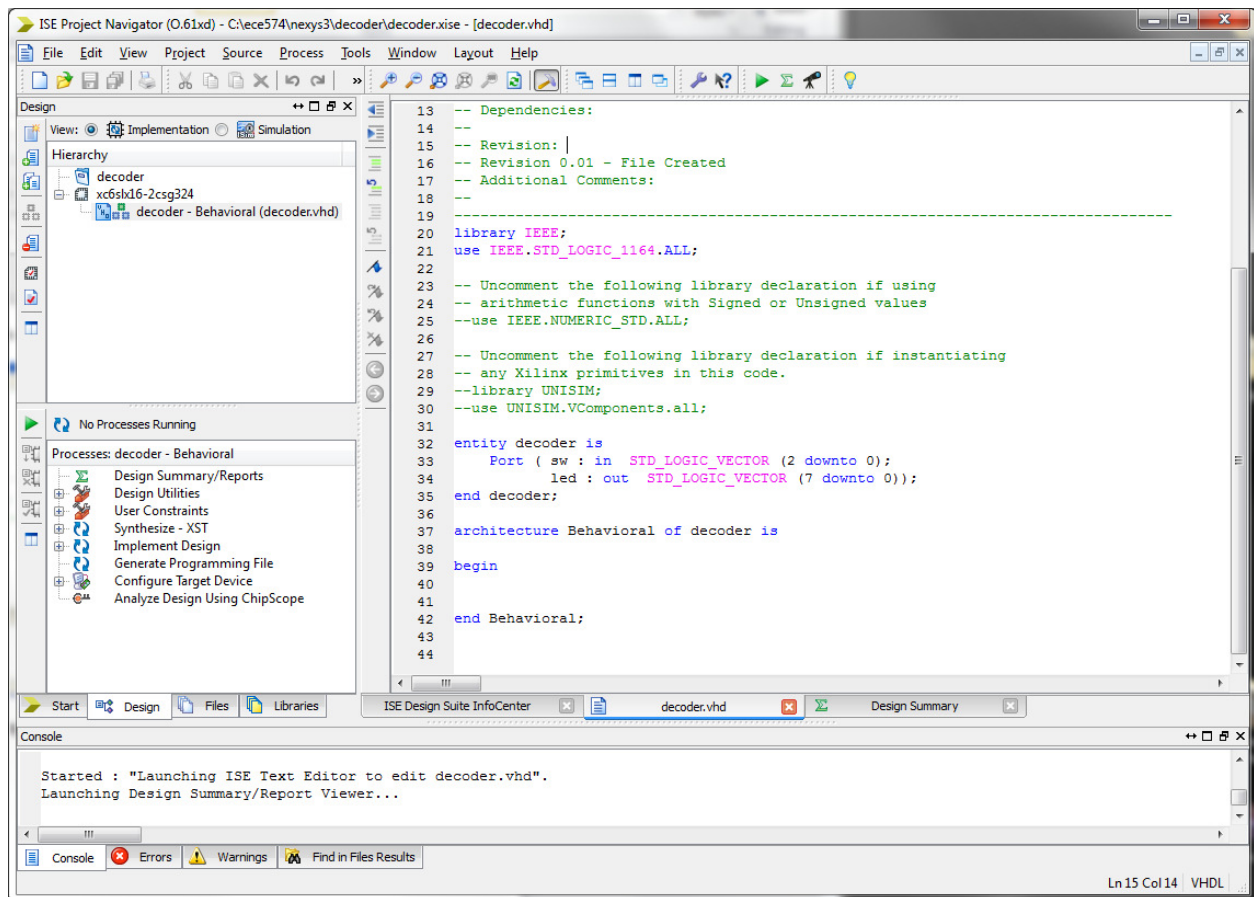
Select *VHDL Module*, and type "decoder" for name:



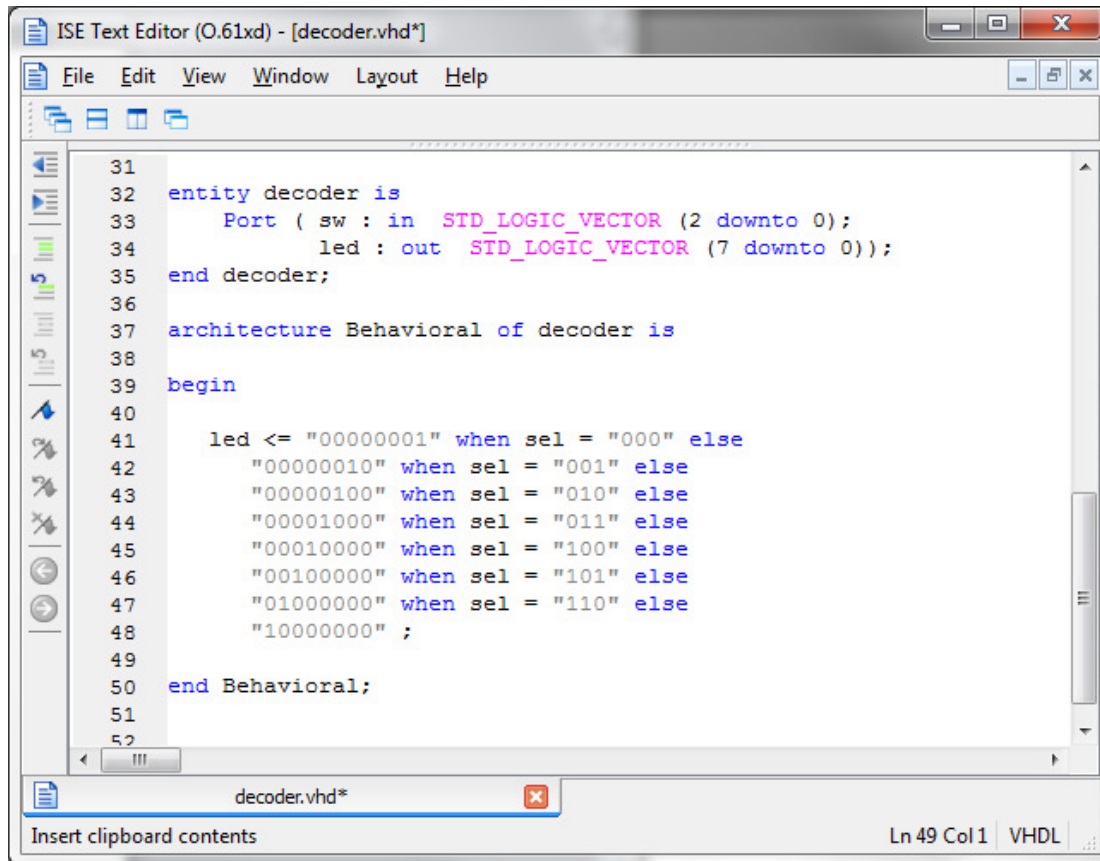
Click **Next**, and add *sw* and *led* port names, select direction, and bus size:



Click **Next**, and then **Finish**. A skeleton of your decoder VHDL source file is open for editing:



Add VHDL statements to describe the operation of the 3 to 8 decoder:

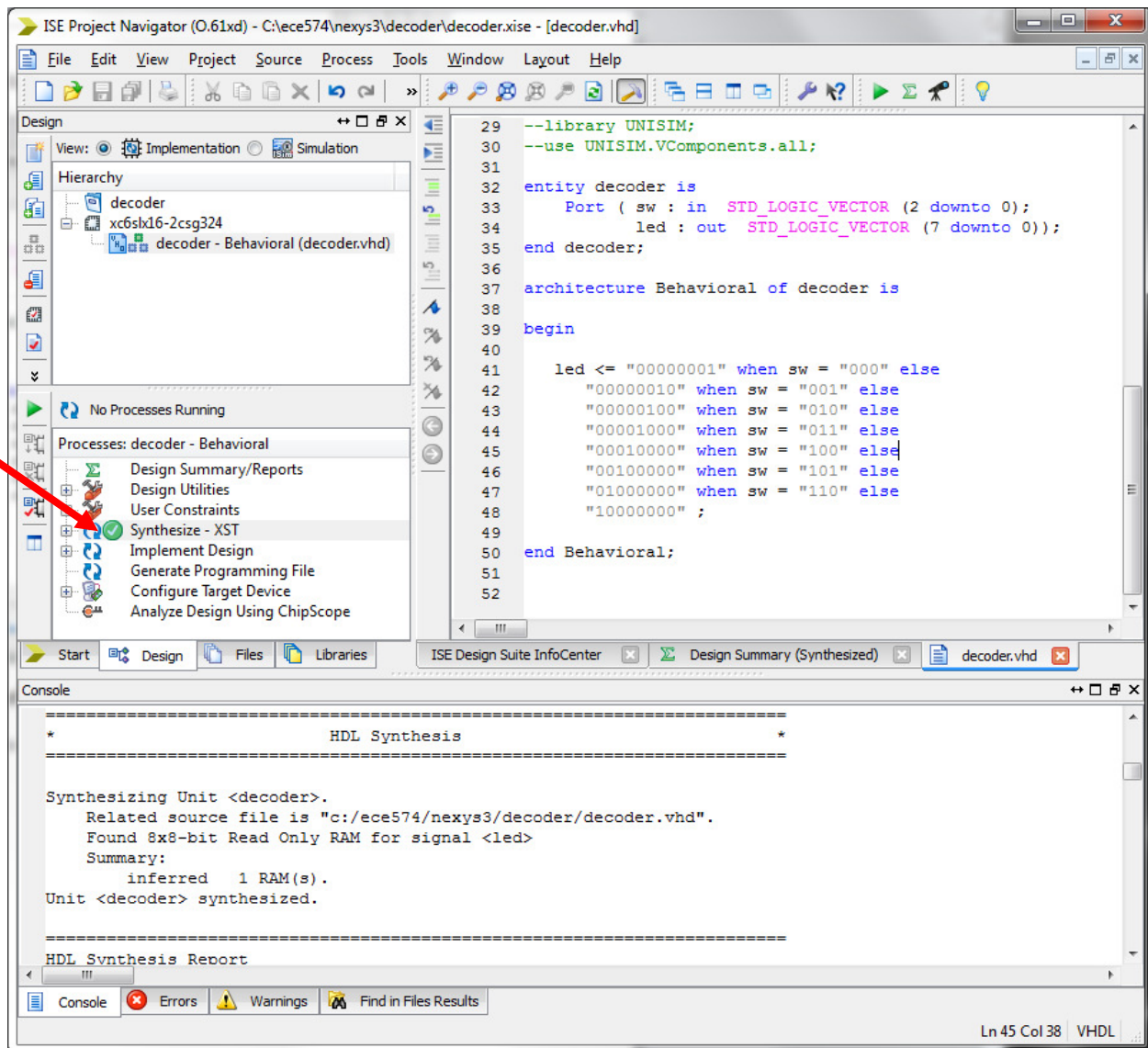
The screenshot shows the ISE Text Editor window titled "ISE Text Editor (O.61xd) - [decoder.vhd*]". The menu bar includes File, Edit, View, Window, Layout, and Help. The code is as follows:

```
31  
32 entity decoder is  
33     Port ( sw : in  STD_LOGIC_VECTOR (2 downto 0);  
34           led : out STD_LOGIC_VECTOR (7 downto 0));  
35 end decoder;  
36  
37 architecture Behavioral of decoder is  
38 begin  
39  
40     led <= "00000001" when sel = "000" else  
41           "00000010" when sel = "001" else  
42           "00000100" when sel = "010" else  
43           "00001000" when sel = "011" else  
44           "00010000" when sel = "100" else  
45           "00100000" when sel = "101" else  
46           "01000000" when sel = "110" else  
47           "10000000" ;  
48  
49 end Behavioral;  
50  
51  
52
```

The status bar at the bottom indicates "Ln 49 Col 1" and "VHDL".

In the Processes window (middle-left window of ISE Project Navigator) – double-click on Synthesize to verify your design.

If successful you should see a green check mark next to the Synthesize operation:



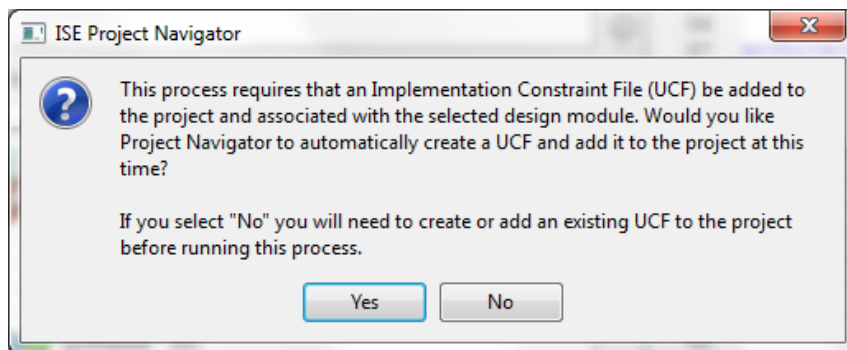
Note: in the Console window note that 1 RAM is inferred.

Note: If any syntax errors are listed then fix these in your *decoder.vhd* source file.

We now need to assign FPGA pins to the switches and leds so they will be connected to the correct ports on the board. This is done by creating a UCF file (User Constraints File).

Expand the *User Constraints* process in the Processes window and double-click on the **I/O Pin Planning (Plan Ahead) - Post Synthesis**.

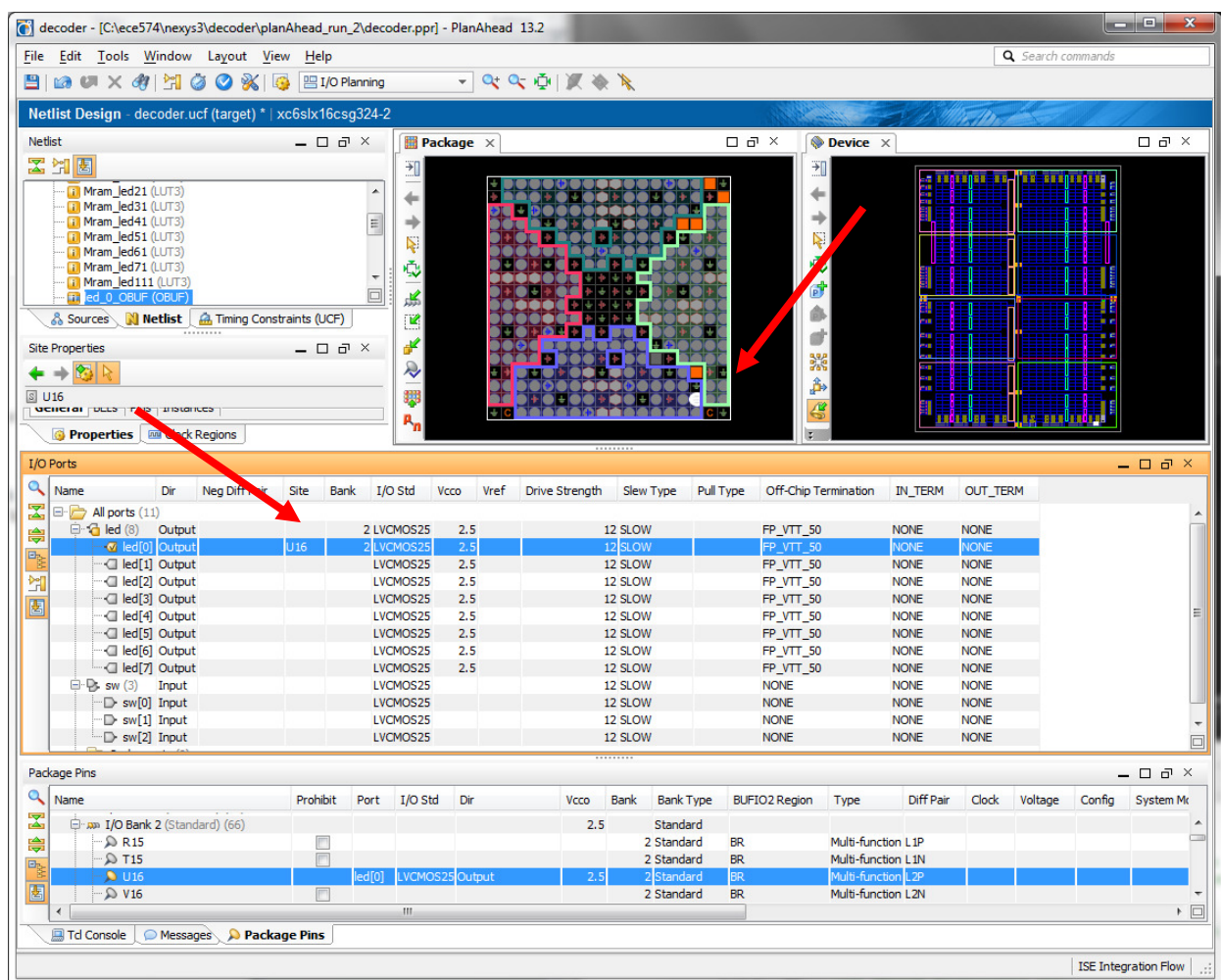
Plan Ahead will start and alert you to create a UCF file:



Select Yes

PlanAhead will now run, eventually a window will open (select the I/O ports tab and then expand the led and sw ports).

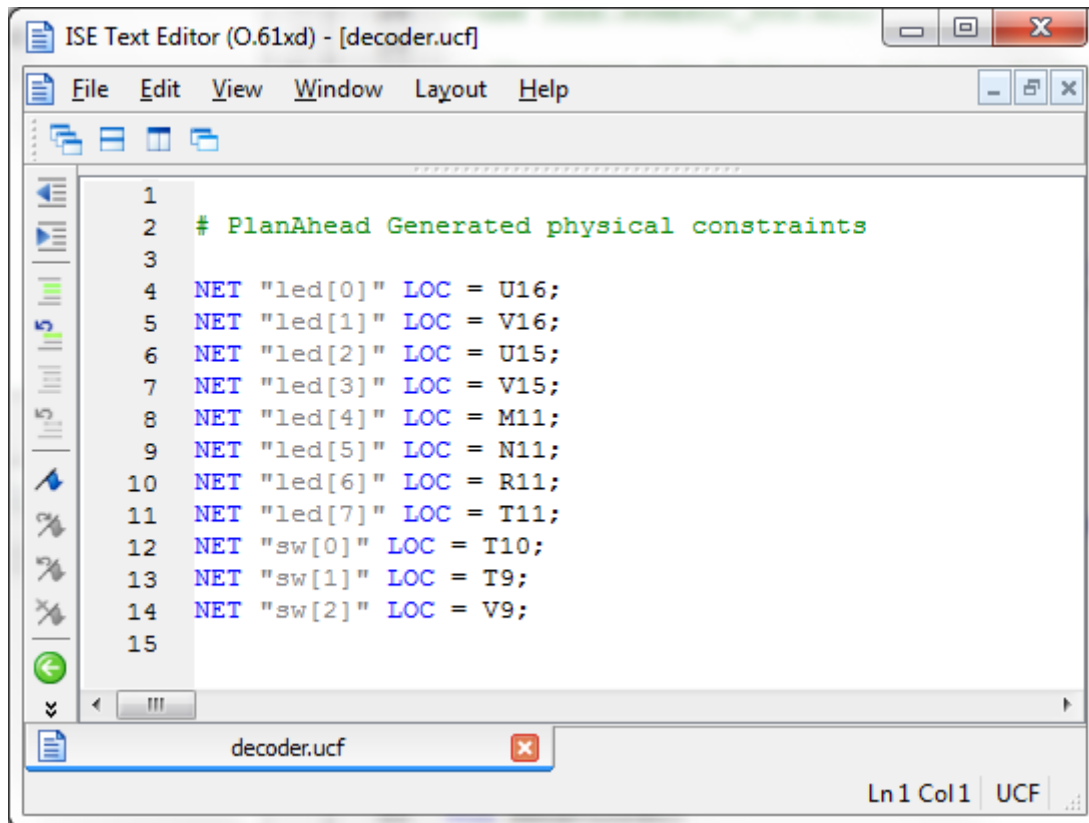
Select led[0] in the I/O ports window and drag to the package pin location U16:
The Site box in the I/O Port Properties window should be updated (instead of dragging, you can also type the site location directly).



With reference to the Nexys3 Reference Manual complete the pin information for the rest of the led and sw ports.

Select **File => Save Design** and exit PlanAhead.

In the ISE Project Navigator Design - Hierarchy window expand the decoder and you should see the new decoder.ucf file is now added. To view the UCF file, select the *decoder.ucf* and then select **Edit Constraints** (Text) in the Processes window and the *decoder.ucf* file will open:



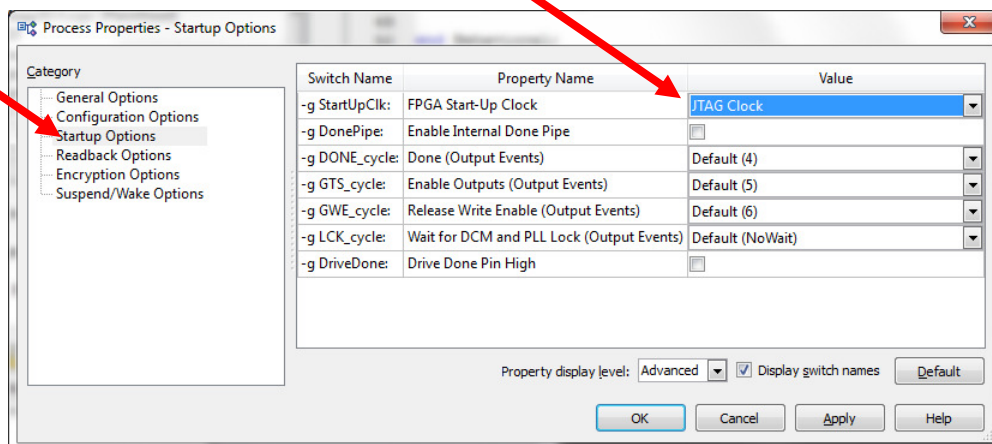
Note: You can also just create and edit this UCF file using a text editor (like Notepad or wordpad).

We can now complete the Synthesis, Implementation, and Generate Programming File steps.

When we generate a programming file we need to specify the FPGA Startup Clock. This will be set to JTAG for when we load the FPGA through the USB connector using the Adept Programming Software. When we generate a PROM (FLASH) file then the startup clock should be set to CCLK.

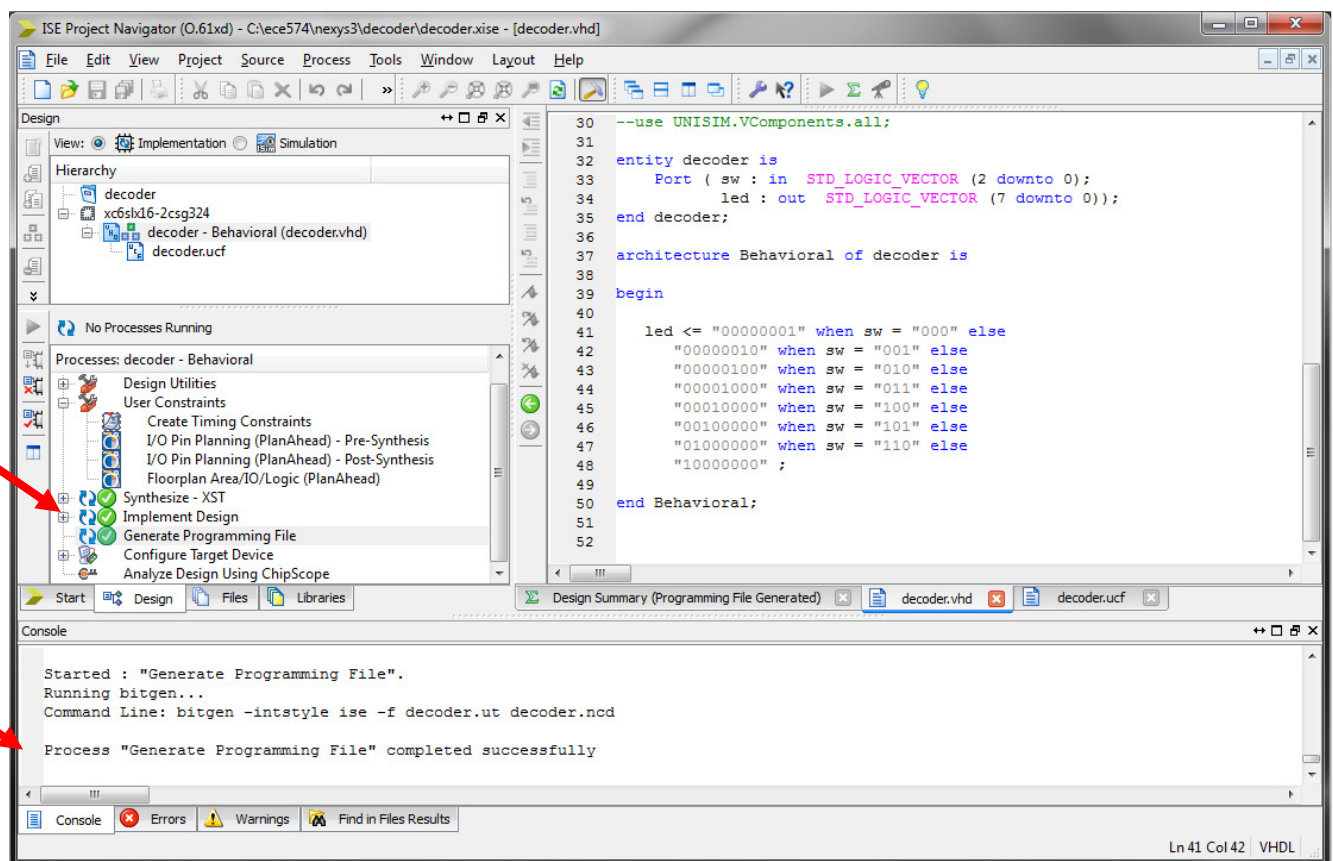
To set the start-up clock, right-click on the *Generate Programming File* in the *Processes* window and then select *Process Properties*.

Select the *Startup Options* in the Category window and change to JTAG (for loading via USB):



Back in the design window select the decoder-Behavioral (decoder.vhd) and then double-click on the **Generate Programming File** process.

You should eventually see a "Generate Programming File" message in the console window and green check marks against Synthesis, Implementation, and Generate Programming File processes:



Select the *Design Summary Properties* tab in the emain window and you can view the FPGA device utilization and other results:

The screenshot shows the ISE Project Navigator with the 'Design Summary (Programming File Generated)' tab selected. The left pane shows the project hierarchy with 'decoder.vhd' selected. The main window displays the 'decoder Project Status (08/27/2011 - 19:32:43)' and 'Device Utilization Summary'.

decoder Project Status (08/27/2011 - 19:32:43)				
Project File:	decoder.xise	Parser Errors:	No Errors	
Module Name:	decoder	Implementation State:	Programming File Generated	
Target Device:	xc6slx16-2csg324	Errors:	No Errors	
Product Version:	ISE 13.2	Warnings:	No Warnings	
Design Goal:	Balanced	Routing Results:	All Signals Completely Routed	
Design Strategy:	Virtex Default (unlocked)	Timing Constraints:		
Environment:	System Settings	Final Timing Score:	0 (Timing Report)	

Device Utilization Summary				
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	0	18,224	0%	
Number of Slice LUTs	4	9,112	1%	
Number used as logic	4	9,112	1%	
Number using O6 output only	0			
Number using O5 output only	0			
Number using O5 and O6	4			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number of occupied Slices	3	2,278	1%	
Number of LUT Flip Flop pairs used	4			
Number with an unused Flip Flop	4	4	100%	
Number with an unused LUT	0	4	0%	
Number of fully used LUT-FF pairs	0	4	0%	
Number of slice register sites lost to control set restrictions	0	18,224	0%	
Number of bonded IOBs	11	232	4%	
Number of IOB-Ced IOBs	11	11	100%	
Number of RAMB16B16s	0	32	0%	
Number of RAMB8B16s	0	64	0%	

Some of this information and also from the corresponding *Design Overview* files will be required for your project reports.

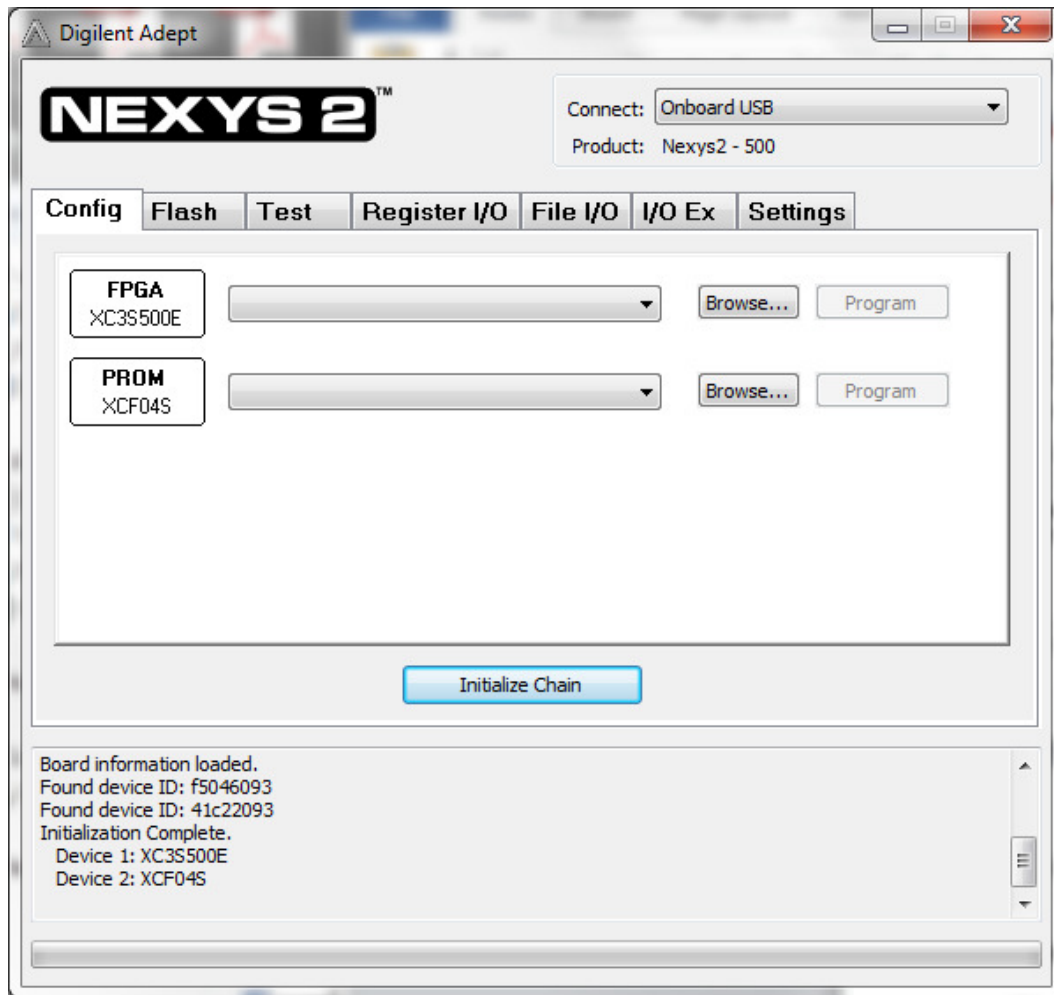
You can now close the ISE Project Navigator.

Loading the FPGA

The next step is to transfer the FPGA bit file through the USB cable using the Digilent Adept software (download from the Digilent website and install).

Connect your Nexys2/3 board to a USB connector on the PC.

Click on the Adept software and the Adept software should recognize the board and show the FPGA and PROM devices:



(Select **Initialze Chain** if you do not see the FPGA and PROM devices)

On the FPGA line select *Browse* and select the *decoder.bit* file from your project directory

Then select **Program**.

After programming the DONE led should light on your board and your design should start running!

You can also load a bit file into the PROM (remember to change the startup clock to CCLK).