Creating a Project using Xilinx ISE 14.7: A Half Adder Circuit using Schematic Capture

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1 Introduction

The objective of this tutorial is to familiarize the student with the Xilinx ISE Design Suite 14.7. This software package provides the digital designer with a wide variety of software tools. These allow digital circuits to be designed and simulated before they are implemented in hardware. CAD tools such as these are essential for designing complex digital circuits. They remove much of the drudgery from the design process and allow the designer to concentrate on the creative part of the design. In this tutorial you will learn the following topics:

1. How to use the Xilinx Foundation Design Suite.
2. How to enter your design using Schematic Capture, and create a symbol.
3. How to synthesize, implement your design.
4. How to reconfigure the FPGA with your design.

To complete this tutorial, you will need a Nexys 3 FPGA board, a micro USB cable, and access to a computer with the Xilinx Project Navigator software installed.

2 Xilinx ISE 14.7 Tool

The ISE Software controls all aspects of the design flow. Through the Project Navigator interface, you can access all the design entry (Schematic, VHDL) and design implementation tools. You can also access the files and documents associated with your project. By default, the Project Navigator interface is divided into three panel sub-windows:

1. Design Panel, which provides access to the View, Hierarchy, and Process panes. The View pane radio buttons enable you to view the source modules associated with the **Implementation** or **Simulation** Design View in the Hierarchy pane. If you select Simulation, you must select a simulation phase from the drop-down list.
2. Console Panel, which provides all standard output from processes run from the Project Navigator. It displays errors, warnings, and information messages.

3. Workspace panel, is where design editors, viewers, and analysis tools open. These include ISE Text Editor, Schematic Editor, Constraint Editor, Design Summary/Report Viewer.

In this tutorial you will explore the functionality of only a sub-set of the Project Navigator capabilities.

3 Design of Half Adder Circuit

In this section we will implement the half-adder circuit.

Specifications:

The half adder will take in two binary digits in order to produce a sum bit and carry bit.

Define inputs and outputs:

Inputs: two bits (A and B).
Outputs: a sum bit (S) and a carry bit (C).

Create a truth table:

Inputs		Outputs	
A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Derive Boolean equations:

As we can see from the truth table, the carry bit is only set when both A and B are set. This is an AND operation. The sum is set when only one of the two inputs are set. This is an Exclusive-OR operation.

Therefore,

$$C = AB$$
$$S = \overline{A}B + A\overline{B} = A \oplus B$$

We are now ready to enter our design using a CAD tool.

4 Starting a new project

To enter a new design we must first start a new project in the Project Navigator: the main interface for the Xilinx ISE Suite.

1. Load the Project Navigator from the Start Menu:

    → **Xilinx Design tools** → **Project Navigator**.

   A virtual machine running in Oracle VirtualBox will appear. The Project Navigator window will open automatically within the virtual machine.

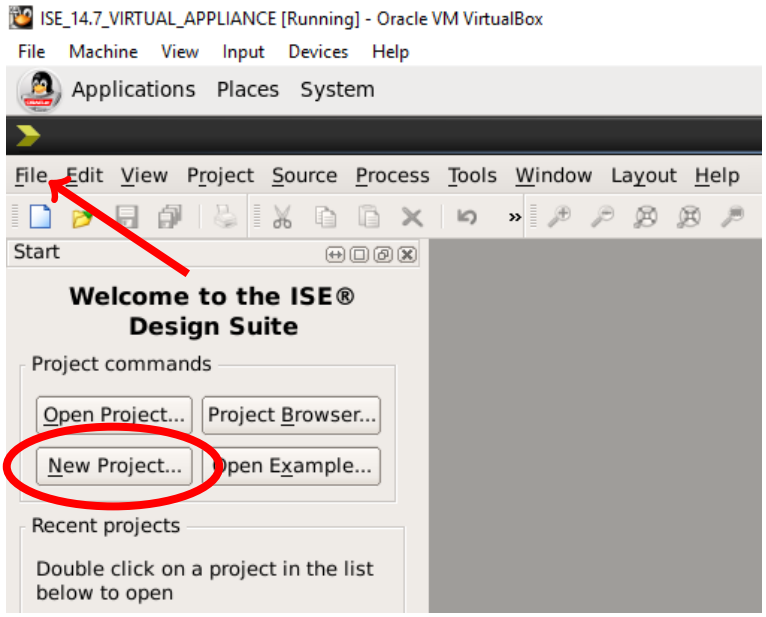

Figure 1: Splash screen in ISE Project Navigator.

2. Click **OK** on the "Tip of the Day" (if shown), then select either **File** → **New Project** or click on the **New Project** tab, shown in Figure 1.

3. The New Project Wizard dialog box will appear. Fill in the fields as shown in Figure 2. For the name, use "SchemCapHalfAdder". Ensure that the top-level source type is "Schematic".

   (Note: As we will need to transfer your project out of the Virtual Machine, you **MUST** set the Location to the Xilinx Share folder located at /home/ise/ISE.)

   When everything is set correctly, click **Next**.

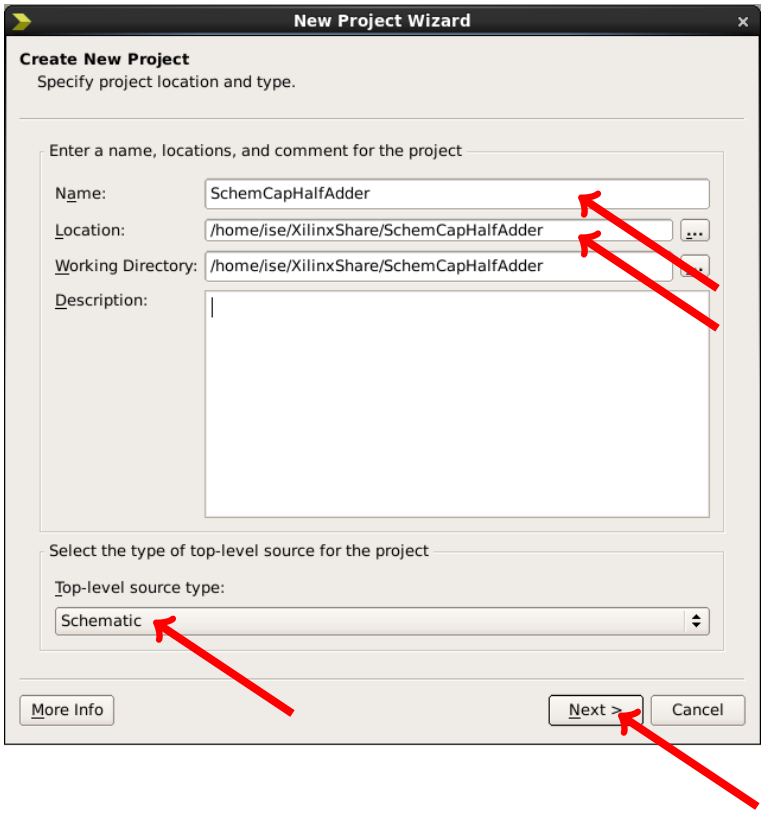

Figure 2: New Project Wizard.

4. Another New Project Wizard dialog box will appear prompting you for device, synthesis and simulation settings for the project.

   In this dialog box verify the following settings:

   - **Family → Spartan6**.
   - **Device → XC6SLX16**.
   - **Package → CSG324**.
   - **Speed Grade → -3**.
   - **Synthesis Tool → XST (VHDL/Verilog)**.
   - **Simulator → ISim (VHDL/Verilog)**.
   - **Preferred Language → VHDL**.

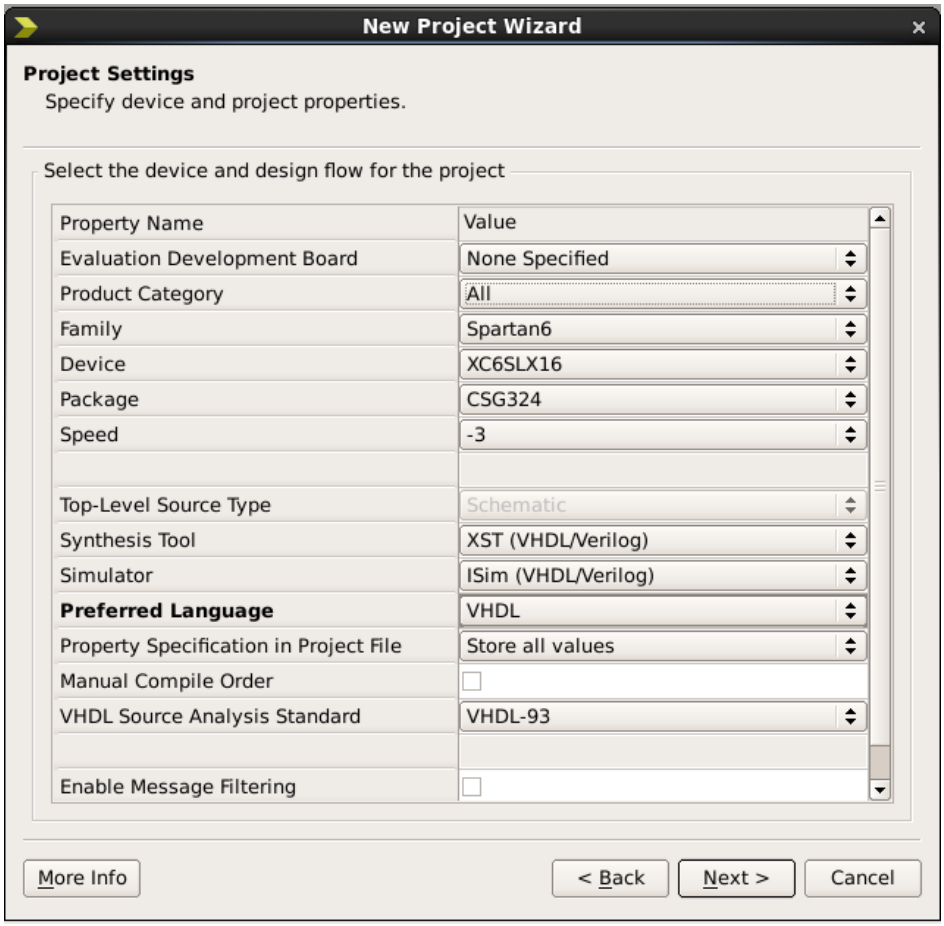

Figure 3: New Project wizard, second screen.

5. If the information is correct click **Next**. The following window will appear: double-check the details and if correct, click **Finish**.

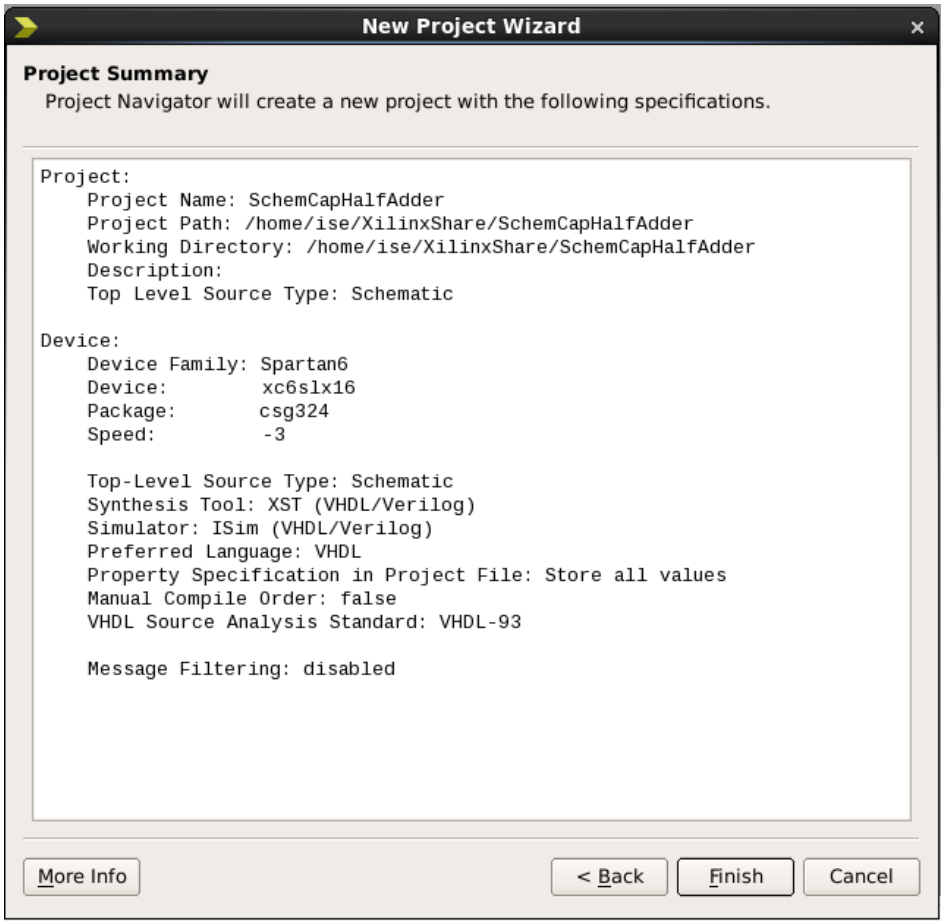

Figure 4: New Project wizard, final screen.

6. Next, we need to create a new Source File and add it to the project. Click on the **New Source** button.

7. In the new dialog box that appears, select **Schematic** from the list of file types and enter "HalfAdderCkt" as the file name.

   The default location is the current project directory and can be left as is. Ensure the **Add to Project** box is selected and click the **Next** button.

   Verify the information in the next dialog box and click **Finish**.

8. If you wish to add an existing source file to the project the Add Existing Sources dialog allows you to do this. Since we are only using new source files in this project we will not worry about this now.

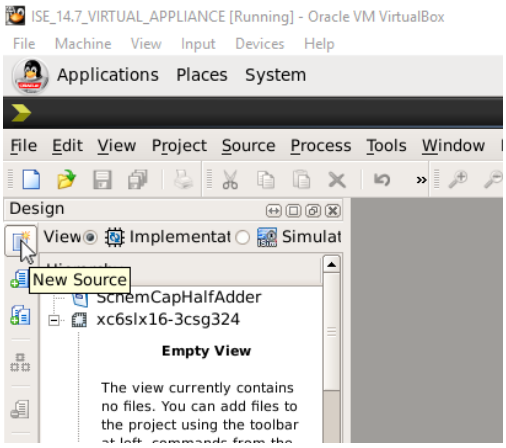

Figure 5: New Source button location.

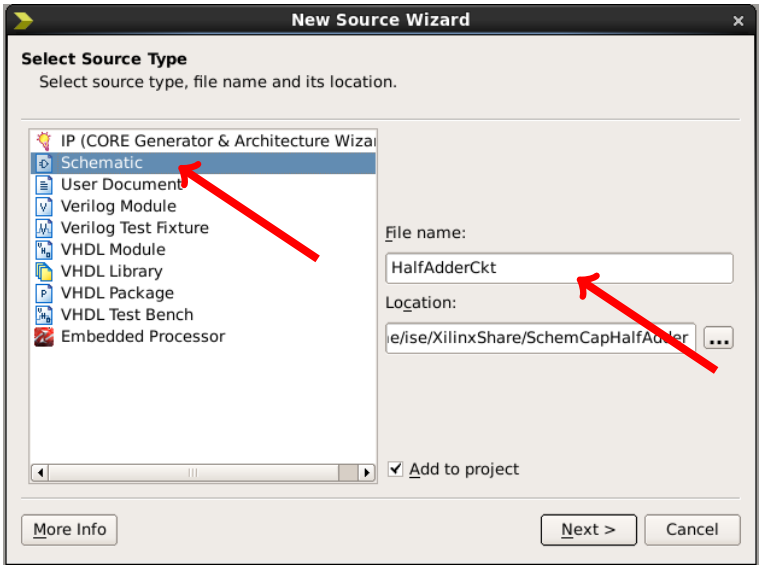

Figure 6: New Source Wizard.

5 Using the Schematic Editor in the Project Navigator

We are now ready to start working with the schematic editor.

1. The Schematic Editor window will have appeared within the Project Navigator interface at the completion of the last step in the previous section.

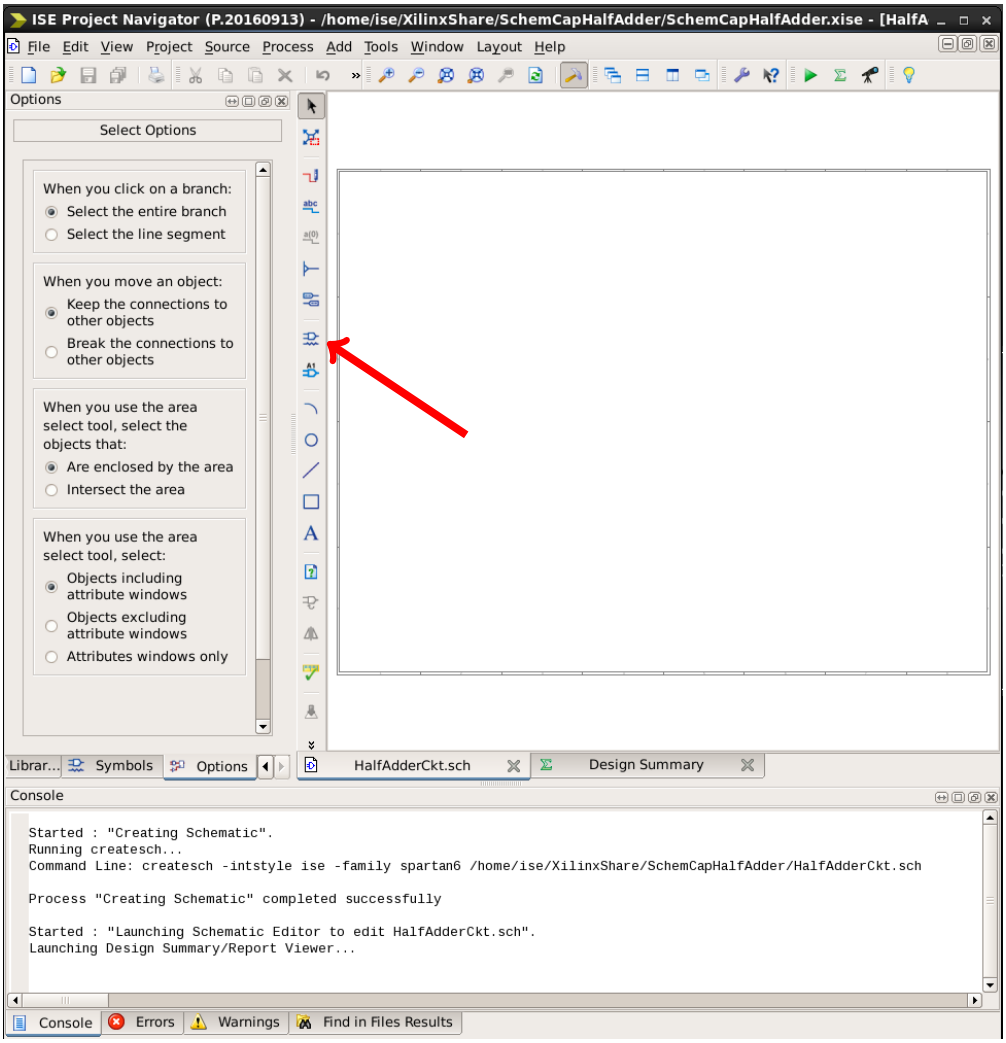

Figure 7: Schematic Capture design entry window; arrow pointing to Add Symbol icon.

2. Now, we insert logic gates into our schematic. Select the  **Add Symbol** icon in the **Options** toolbar. A list of symbol categories will appear on the left hand side of the **Project Navigator** window.

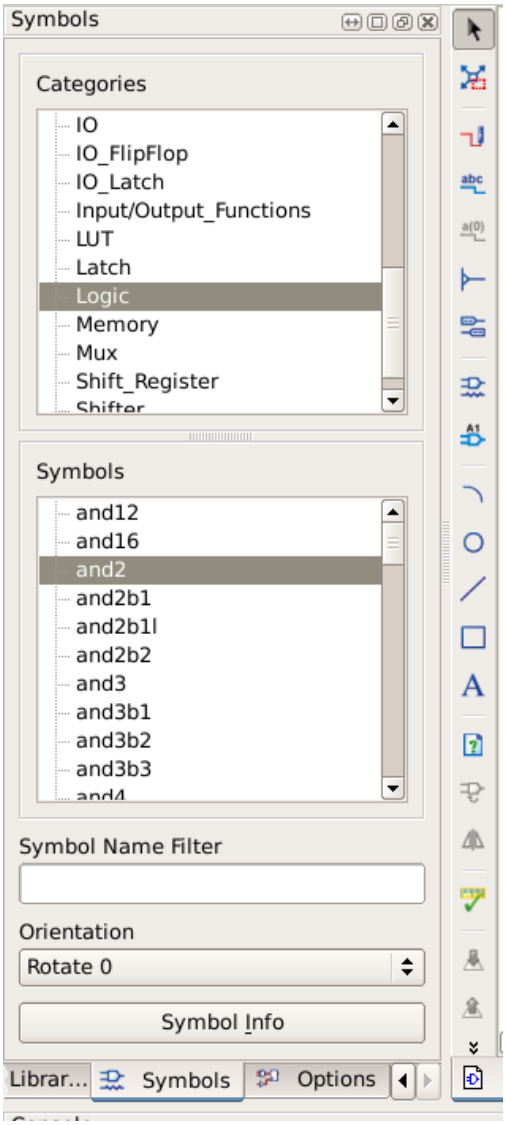

Figure 8: List of symbols available for entry into the schematic.

Select **Logic** from this list and a list of simple logic gates will be shown in the lower **Symbols** scroll box. For the half adder, we will require a 2 input XOR gate and a 2 input AND gate.

To add a simple logic gate to the circuit, left-click to select a symbol from the Symbols list, move the cursor to the Schematic canvas where you want the symbol to be placed, and left-click again to drop the gate in the schematic.

You can also find a symbol by typing a name into the symbol name filter.

3. Now, left click on **AND2** then move your mouse onto the drawing area. You will see the symbol for the AND gate appear. Put it in the desired location and left click the mouse. This

will drop it. Do the same for the XOR gate (XOR2).

Figure 9 highlights the tools necessary for creating a basic digital circuit using schematic capture:

(a) The Magnifying Glass icon indiscriminately zooms to the center of the schematic.

(b) The Zoom Box icon is used to draw a box using the mouse to magnify a specific area of the schematic.

(c) the Add Wire tool icon enters wire mode.

(d) The Add I/O marker tool icon enters the Add I/O Marker mode, allowing you to specify signal entry and exit points for the schematic.

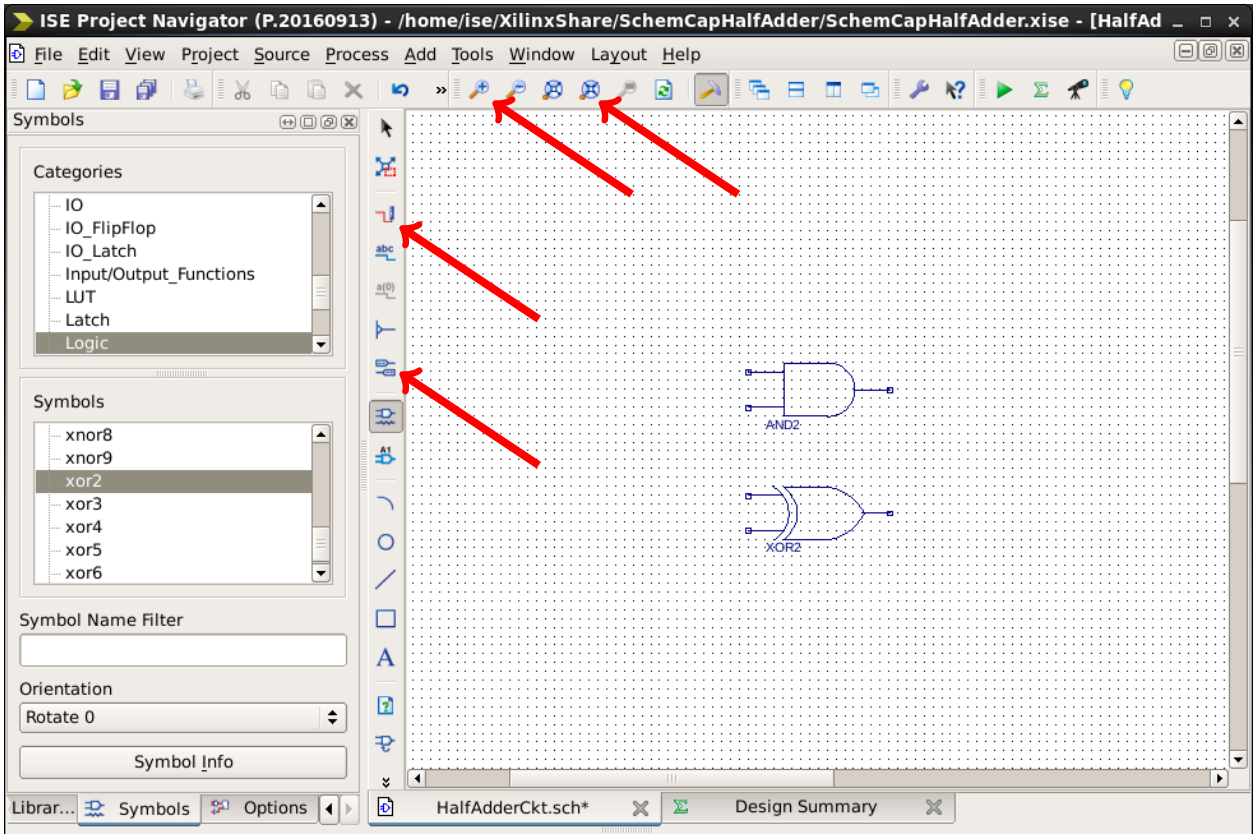

Figure 9: Tools used to create a Schematic Capture design.

4. Next, we need to switch to **Wire** mode to add wires to our circuit. This can be accomplished by:

(a) Clicking on the  button in the vertical schematic toolbar, **or**,

(b) Selecting **Add** → **Wire** in the menu bar, **or**,

(c) Using the Ctrl-W keyboard shortcut, **or**,

(d) Pressing the right mouse button while in the drawing area and select **Add** → **Wire** from the floating menus.

5. Once in **Wire** mode connect the gates by doing the following:

   (a) Place the mouse on a pin of a gate; the shape of the cursor will change.

   (b) Left-click the mouse button.

   (c) Move to the new location that you wish to be connected, and left-click the mouse again.

   A wire will be created between the two desired pins.

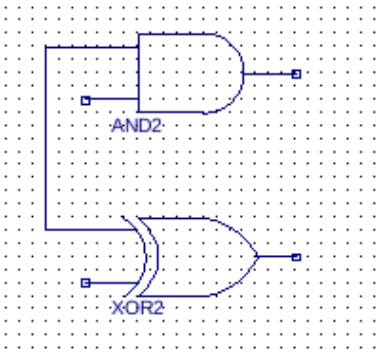

Figure 10: Schematic, after connecting a wire.

6. Useful Hints:

   - To delete a wire or a gate, click on it while in the **Select** mode  and press [Delete].
   - The **Edit** menu contains standard editor functions (undo, select, cut, paste, copy, etc . . .)
   - You will find that you cannot connect two or more wires to an input or output of a gate. Connect the first wire to the gate's connection, then connect additional wires to the first wire.
   - You may also find that the wires will refuse to connect if there are too many wires or gates cluttered together. To solve this, make room for the new wire. Use the **Select** mode to move the wires and the gates around. Click and hold on them then drag them to a new location.
   - To move a gate, you must go back to select mode by either selecting the cursor in the tool bar or pressing the [Esc] key on the keyboard.

7. Next, add a top-level I/O marker to your circuit. These markers tell the synthesizer and simulator tools which ports to regard as overall inputs and outputs.

   To add markers to your circuit, follow these steps:

   (a) Add a wire leading from one of the logic gate inputs to an empty space, creating a "branch end-point". Use [Esc] to exit the tool after creating the wire.

   (b) Left-click the **Add I/O marker** tool icon  to place the cursor into add I/O Marker mode.

   (c) Click on the branch end-point to add an I/O marker.

   Your schematic should look something like Figure 11 (net names may vary).

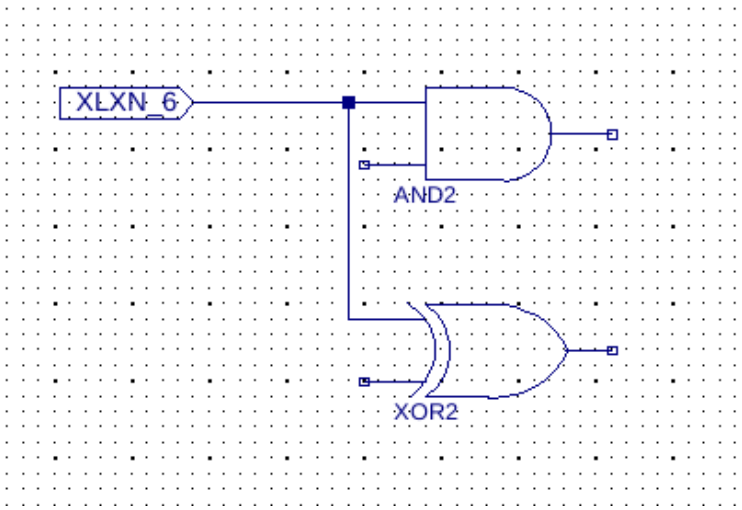

Figure 11: Schematic, after connecting a wire to an I/O marker.

8. Go back to Select Mode  and double left-click on an I/O marker. When the I/O marker's object properties dialog box appears, select the Nets category. In this dialog box, enter a meaningful value for the Name field of the I/O marker, and ensure the port has the proper polarity. The finished dialog box should look similar to Figure 12.

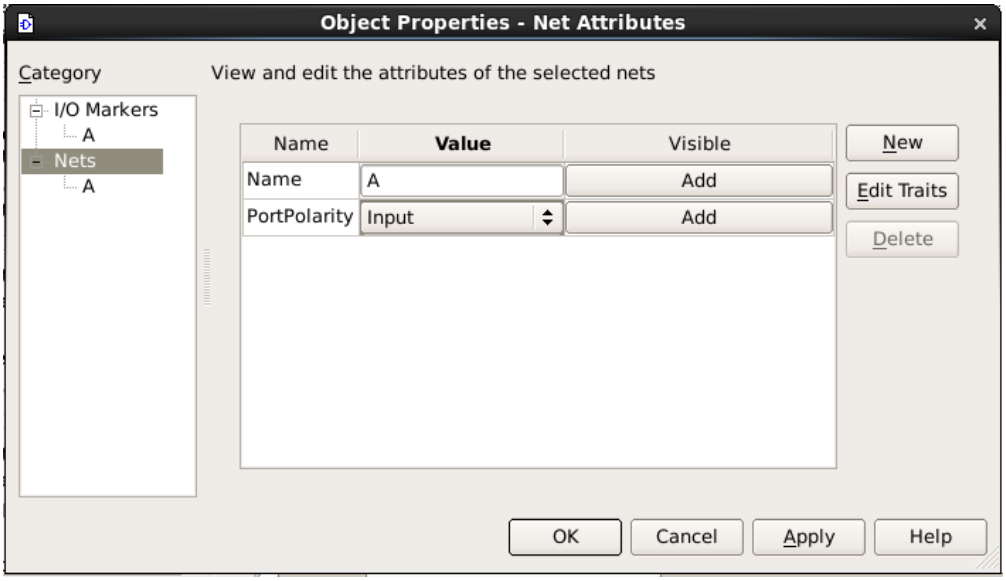

Figure 12: Object Properties dialog box.

Press **Apply** and then **OK**.

9. Repeat this process for all input and output ports (i.e., enter "A" and "B" as inputs, and "S" and "C" as outputs). The finished circuit should look similar to Figure 13.

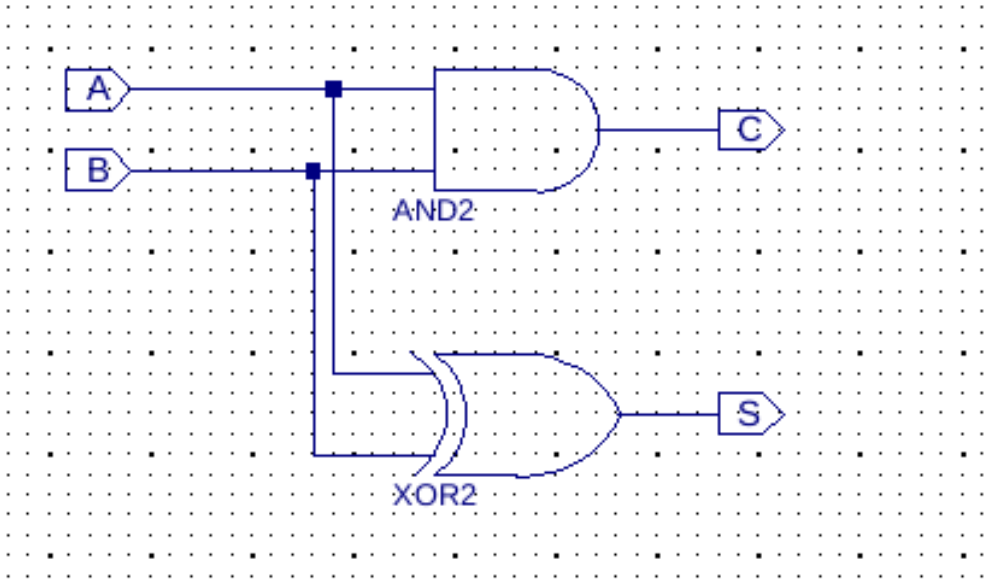

Figure 13: Completed half adder circuit.

10. Next, we add a title. In the **Symbols** tab in the left-hand pane (Figure 14), select **General** in the **Categories** list. In the **Symbols** list below, select **Title**.

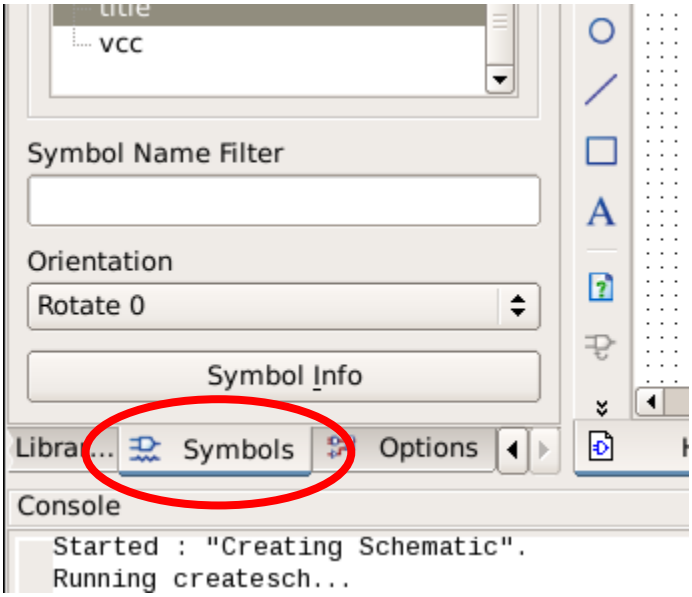

Figure 14: Symbols tab.

Place this symbol in the lower right hand corner of the schematic. To add a title, your name and the date switch to **Select** mode by using the Select tool  to double left-click on the title block symbol in the drawing area. In the Object Properties dialog box that appears change the **Value** field of **TitleFieldText** to "Half Adder" and change **NameFieldText** to an appropriate value. Click **OK**.

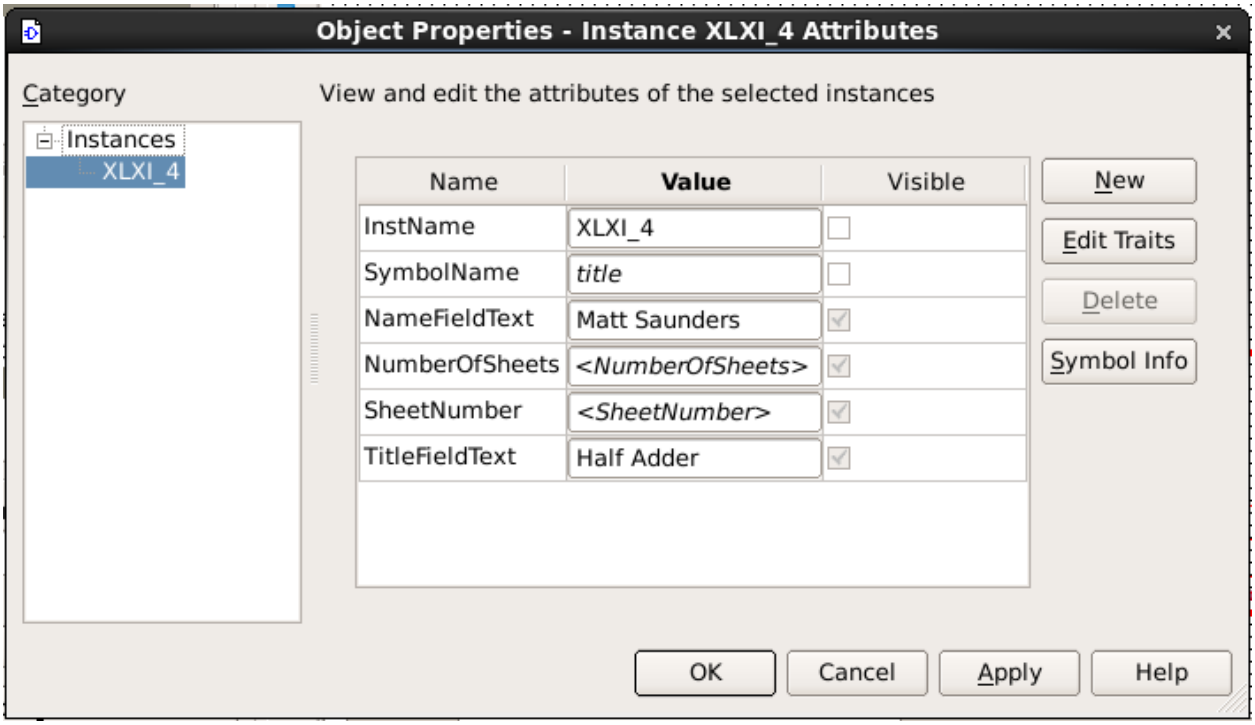

Figure 15: Editing the Title block.

11. We will now check the design for connection errors. In the Menu Bar, select **Tools** → **Check Schematic**. A message will appear in the **Console** window showing error numbers and messages, or if all is well, a "No errors or warning were detected" message will appear. If the test indicates that there are no errors, save your schematic.

We now should have a view as shown in Figure 16.

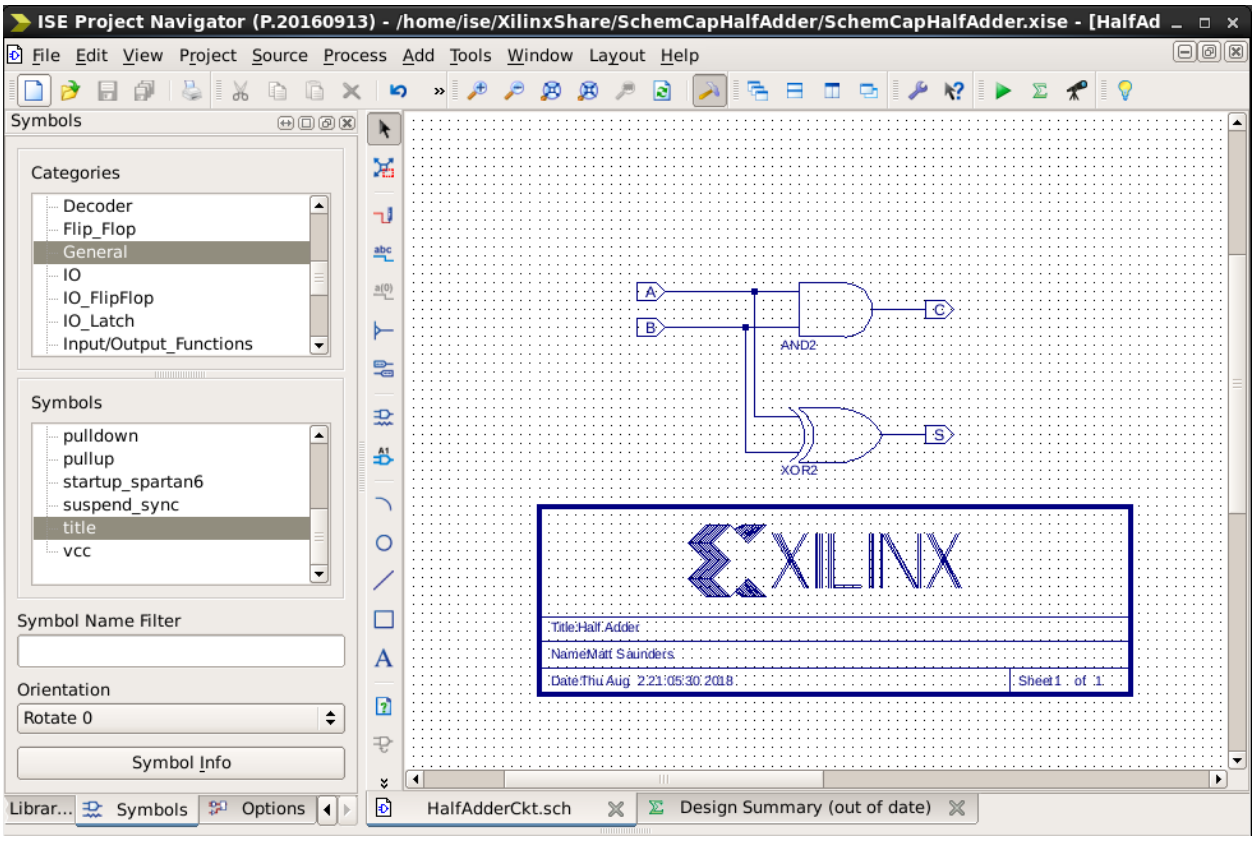

Figure 16: Completed Half Adder block.

We will next create a macro symbol of the half adder to be used in a full adder design.

6 Creating a Macro Symbol for Half Adder

After designing the Half Adder and checking it for connection errors we will create a macro symbol so that we can use it in the design of the Full Adder. To create a macro circuit, follow these steps:

1. Select **Tools** → **Symbol Wizard** from the main menu toolbar. The Symbol Wizard dialog box (figure 17) appears.

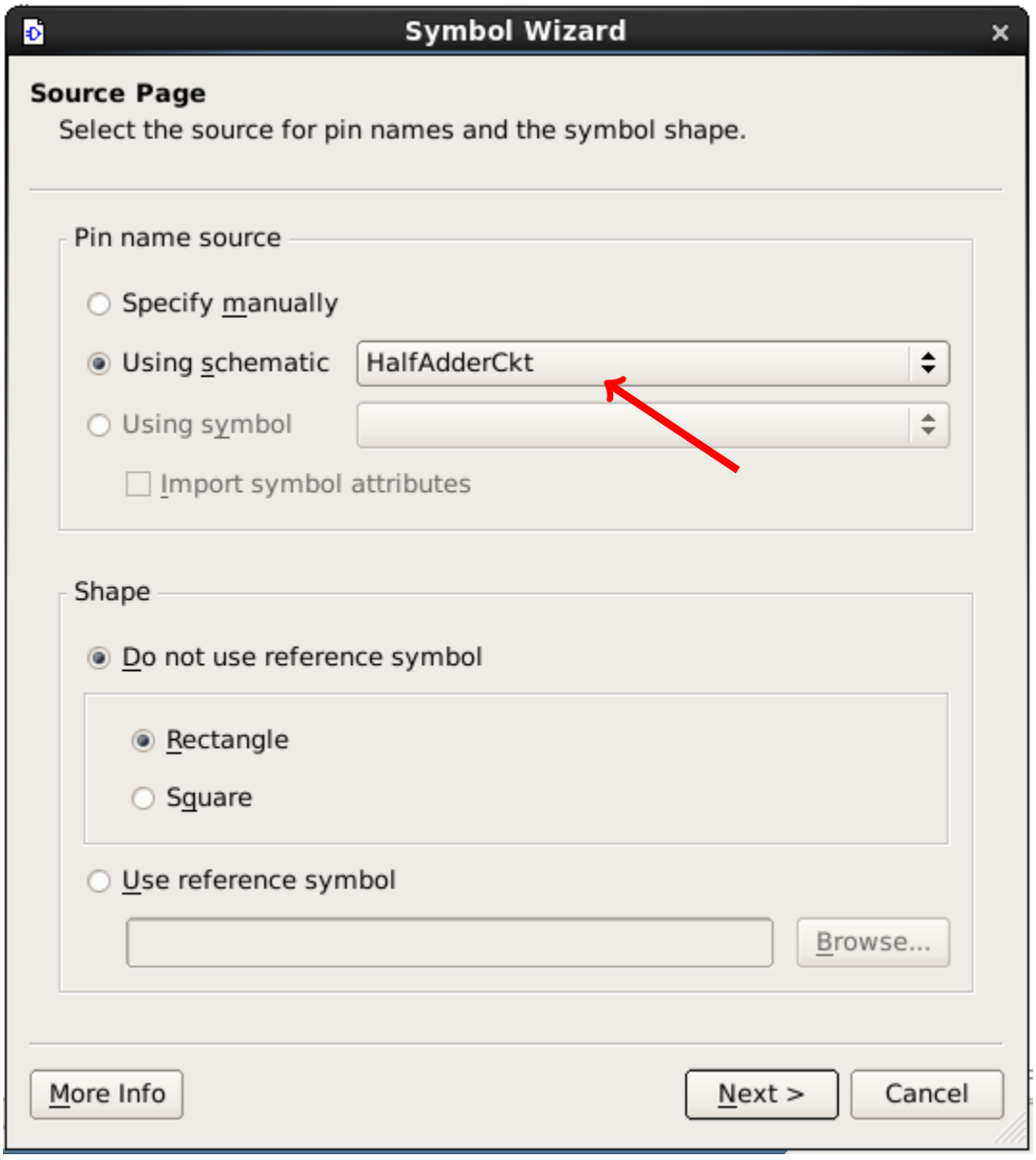

Figure 17: Symbol Wizard dialog box.

2. Under **Pin name source** select **Using Schematic** which defaults to the circuit you just created, HAckt or HalfAdderCkt, depending on how you named your original schematic.

3. Press **Next**.

4. The next dialog box presents general pin placement options that you can modify depending on how you want to name your pins. Press **Next**.

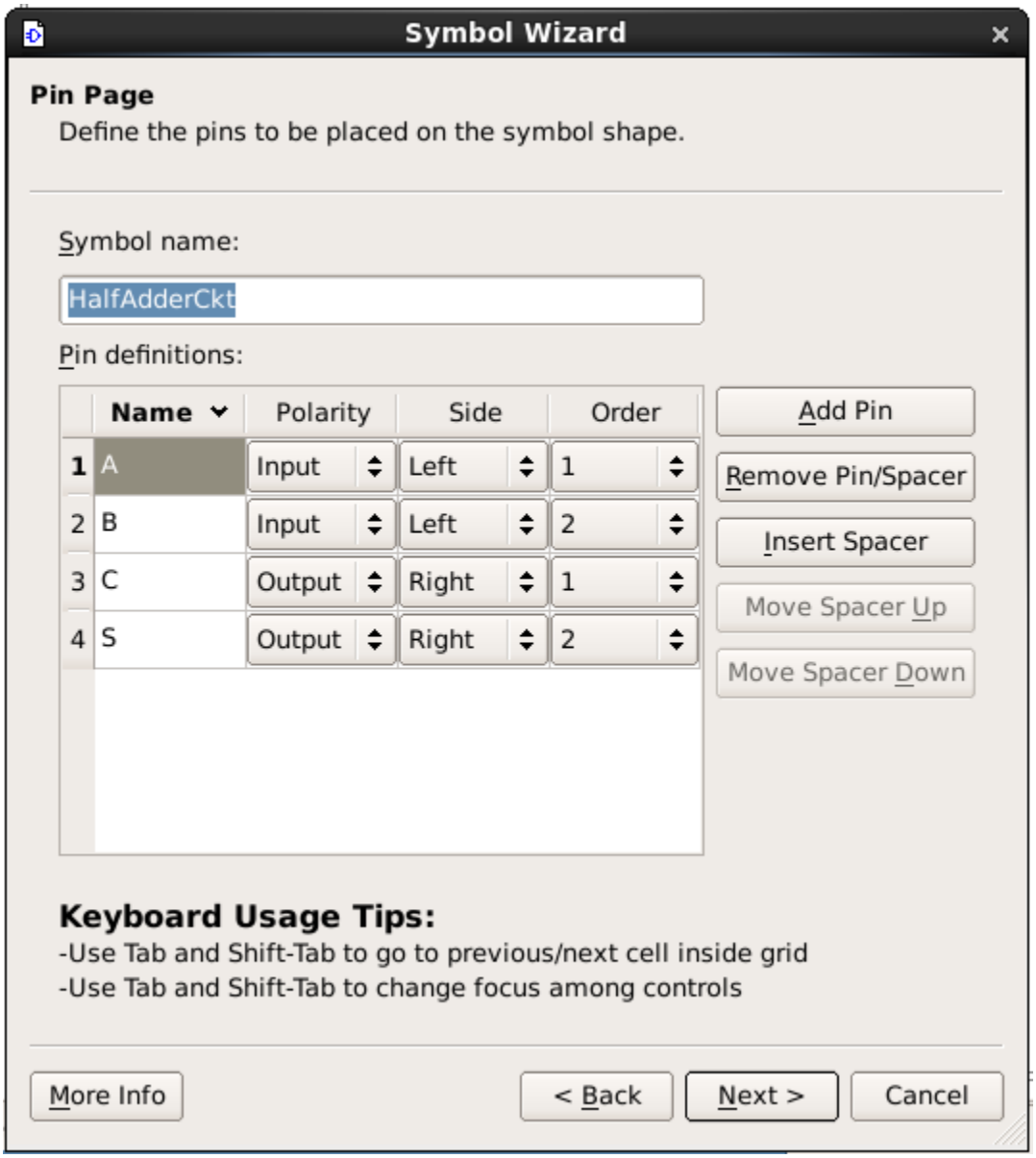

Figure 18: Symbol Wizard pin page.

5. The next dialog box presents symbol size options that you can modify depending on how you want the schematic symbol to appear. Press **Next**.

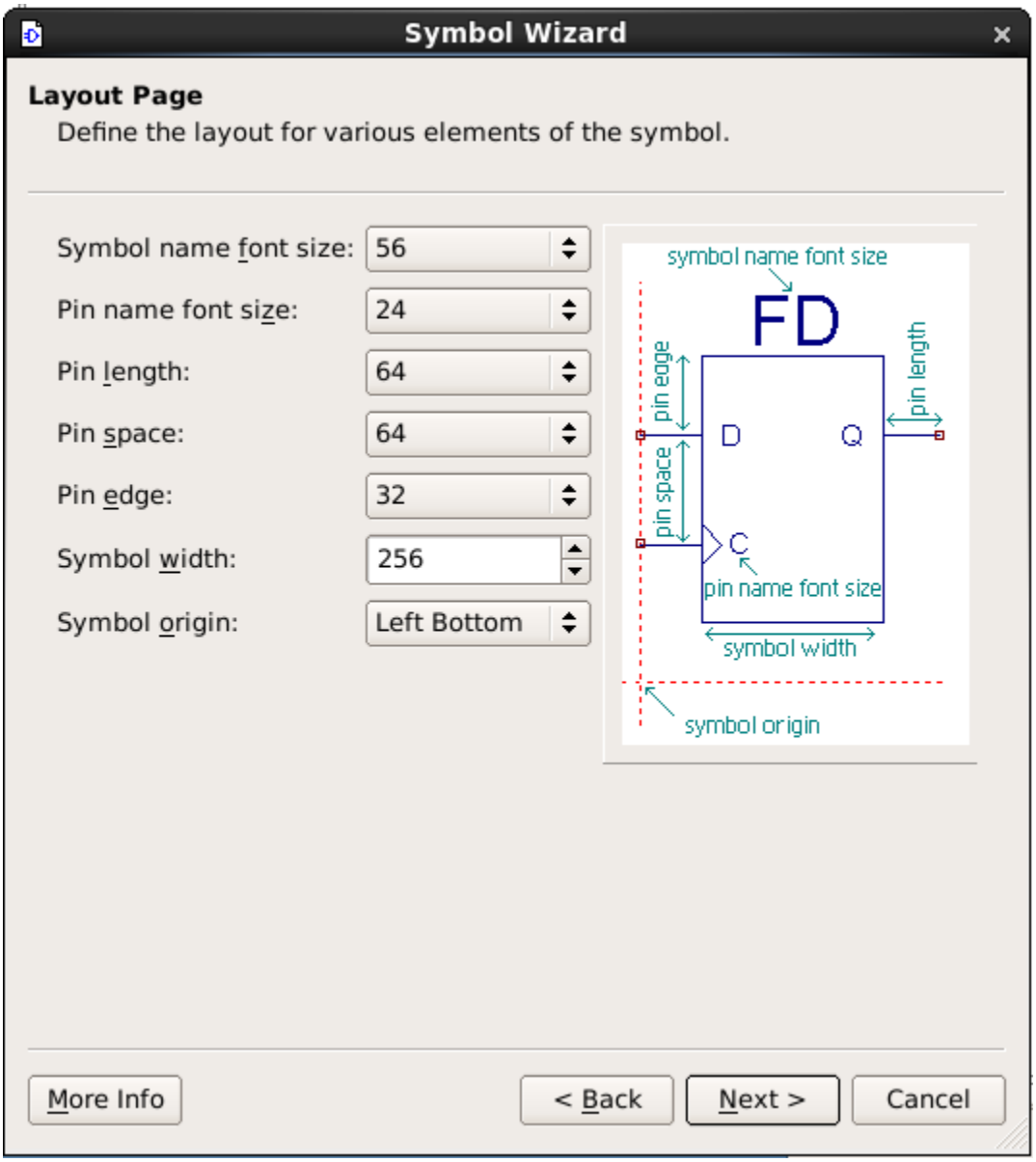

Figure 19: Symbol Wizard layout page.

6. The final dialog box gives you a preview of the symbol, given the settings you've selected. Click **Finish** to finalize the symbol or **Back** to modify the symbol settings.

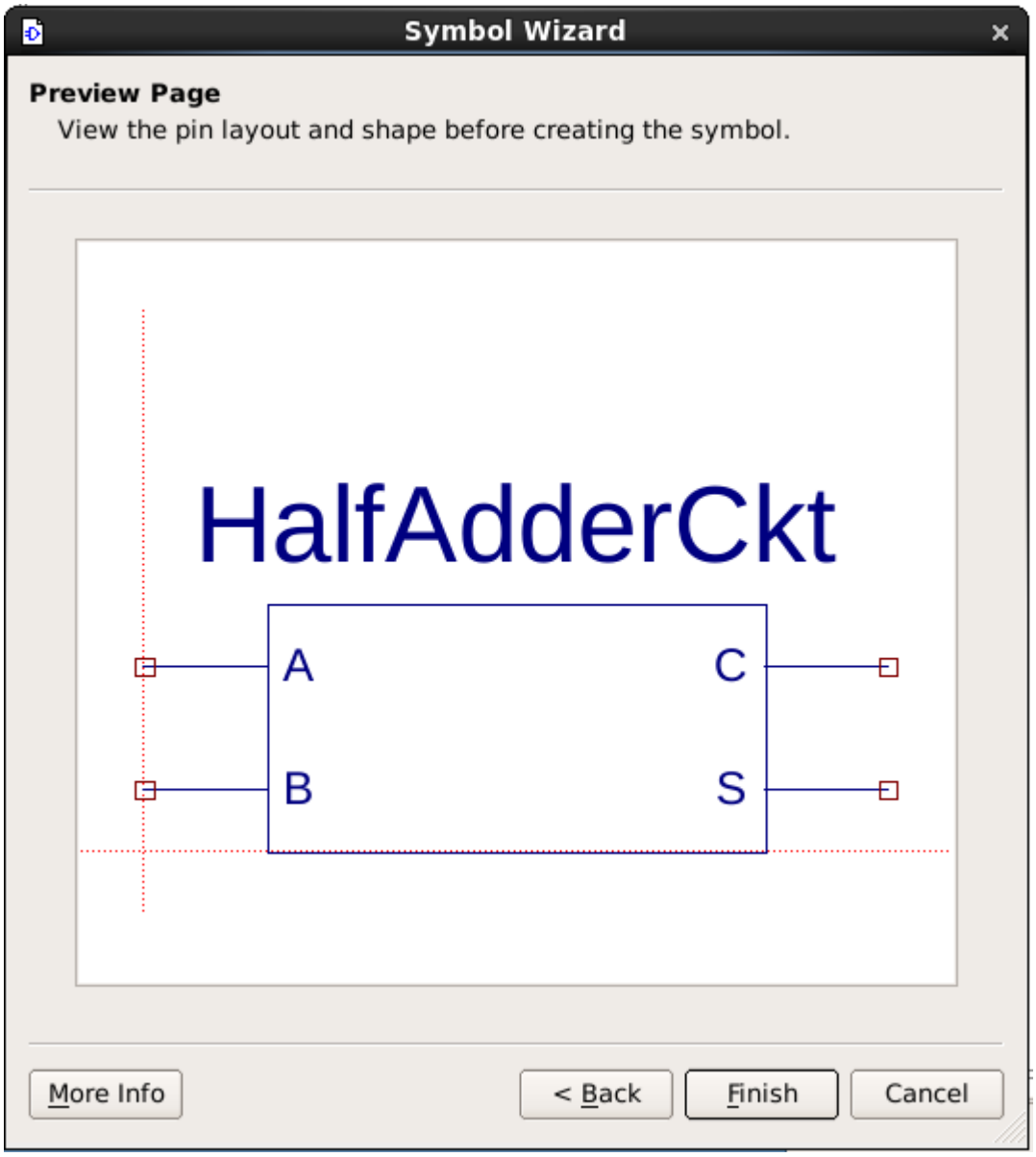

Figure 20: Symbol Wizard layout page.

7. Save all your work. Copy your project files (found in the T:\ISE folder) onto your H drive — otherwise you will lose all your work!

We will next create a UCF file — used to describe the connections between your circuit and the physical components on the Nexys 3 Board.

7 Creating a UCF File

A **U**ser **C**onstraint **F**ile (**UCF**) is used to assign I/O pins in a design to the actual pins on the FPGA.

Please refer to **Appendix B** for more information.

1. Click on the Design tab in the left-side pane.
2. Right-click on the schematic source **HalfAdderCkt.sch** in the Hierarchy pane of the Project Navigator and select **New Source** from the floating menu.
3. From the list of file types select **Implementation Constraints File**. Name the file "HalfAdder_UCF".

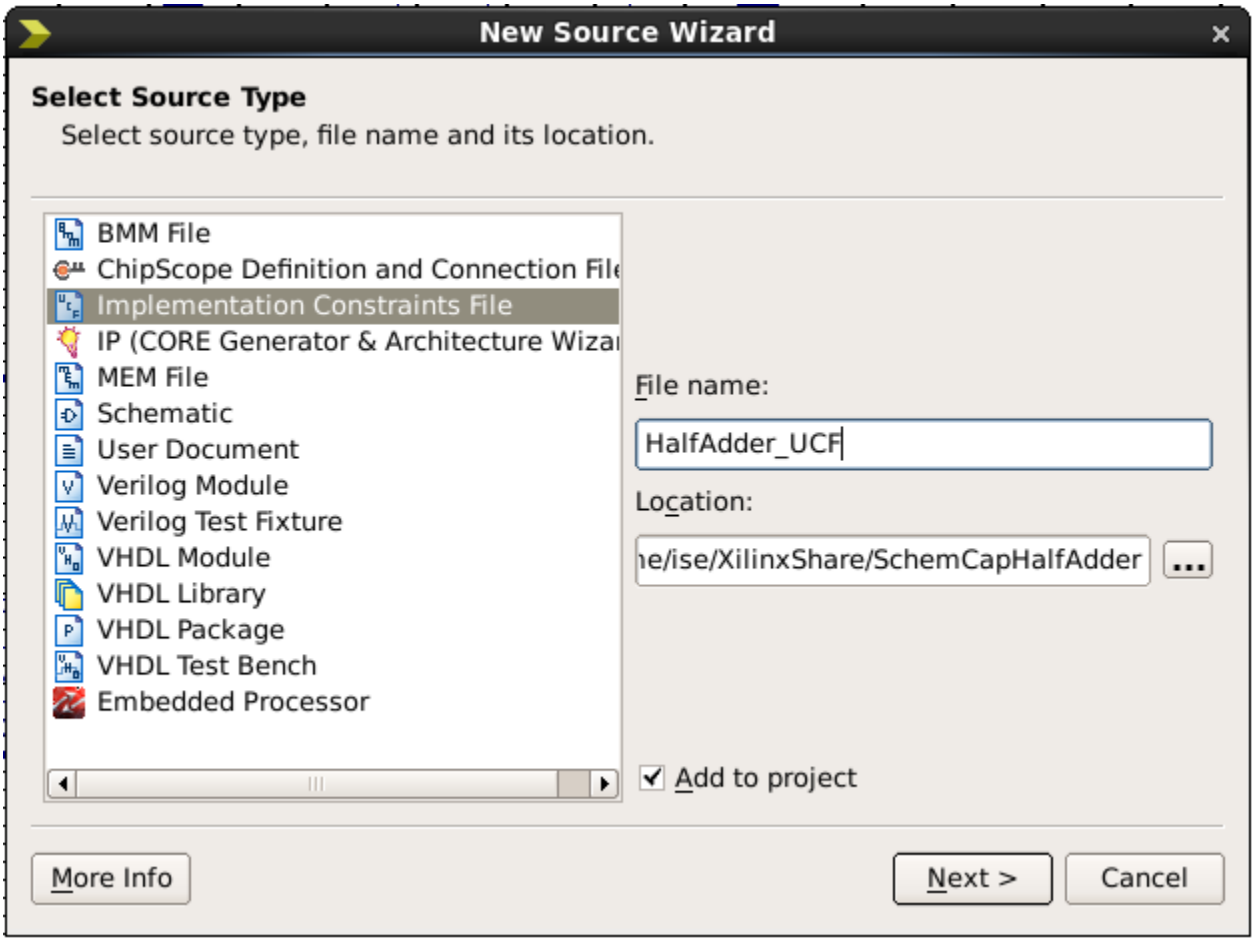

Figure 21: New Source dialog for UCF file.

4. Ensure the **Add to Project** box is selected, then click **Next**.

5. The final dialog box is for confirming the information input in the previous dialog boxes. Click **Finish** if the information is correct.

6. A blank UCF file should open. If not, open it by expanding the HalfAdderCkt menu entry in the Hierarchy pane of the Design tab, then double-clicking on the UCF file.

   The UCF file has the following format:
   `NET` <*pin name in Schematic design*> `LOC=`<*pin number on FPGA*>

   NOTE: Make sure to use upper case letters for the pin names.

7. Let us assign the inputs to the toggle switches on the NEXYS board and the outputs to the LEDs. Please refer to the NEXYS 3 board schematic for more information about pin connections.

   We will connect **A** to Switch 1 (SW1), **B** to Switch 0 (SW0), **S** to LED 0 (LD0) and **C** to LED 1 (LD1).

   For quick reference, each pin connection is silk-screened next to the peripheral on the board itself. For further information about FPGA pins and their attached peripherals check the link "NEXYS 3 Board Pins (FOR UCF FILE ASSIGNMENT)" on the web.

—Design pin	—FPGA pin	—Description
A	T9	SW1
B	T10	SW0
S	U16	LD0
C	V16	LD1

8. Enter the following statements in the **Workspace** panel:

```
NET A LOC = T9;
NET B LOC = T10;
NET S LOC = U16;
NET C LOC = V16;
```

9. You can now save and close the file by pressing **File** → **Save**.

You can get a better idea of our setup by looking at the Digilent NEXYS 3 Programmer's model in **Appendix B**. We will look at this setup in more detail in the following tutorials.

8 Generating a Bit Stream: Compiling the Design

Hitherto, we have examined how to design a digital circuit using the Xilinx ISE Design Suite 14.7 Software. We will now look at how to compile (generate the bit-stream) and download the design to the Digilent NEXYS 3 board.

1. Now go back to the Project Navigator window. Under the Design tab, highlight **HalfAdder-Ckt.sch** in the Hierarchy pane. In the Processes pane, double-click on **Synthesize - XST** to synthesize the design.

   When the synthesis stage has completed, you will see on the console panel:
   `Process "Synthesize - XST" completed successfully`

2. Next, Left double-click Implement Design to implement the design.

   When the implement stage has completed successfully you will see the following message on the console panel:
   `Process "Generate Post-Place & Route Static Timing" completed successfully`

3. Right click on Generate Programming File and choose Process Properties. A window (Figure 22 will appear.

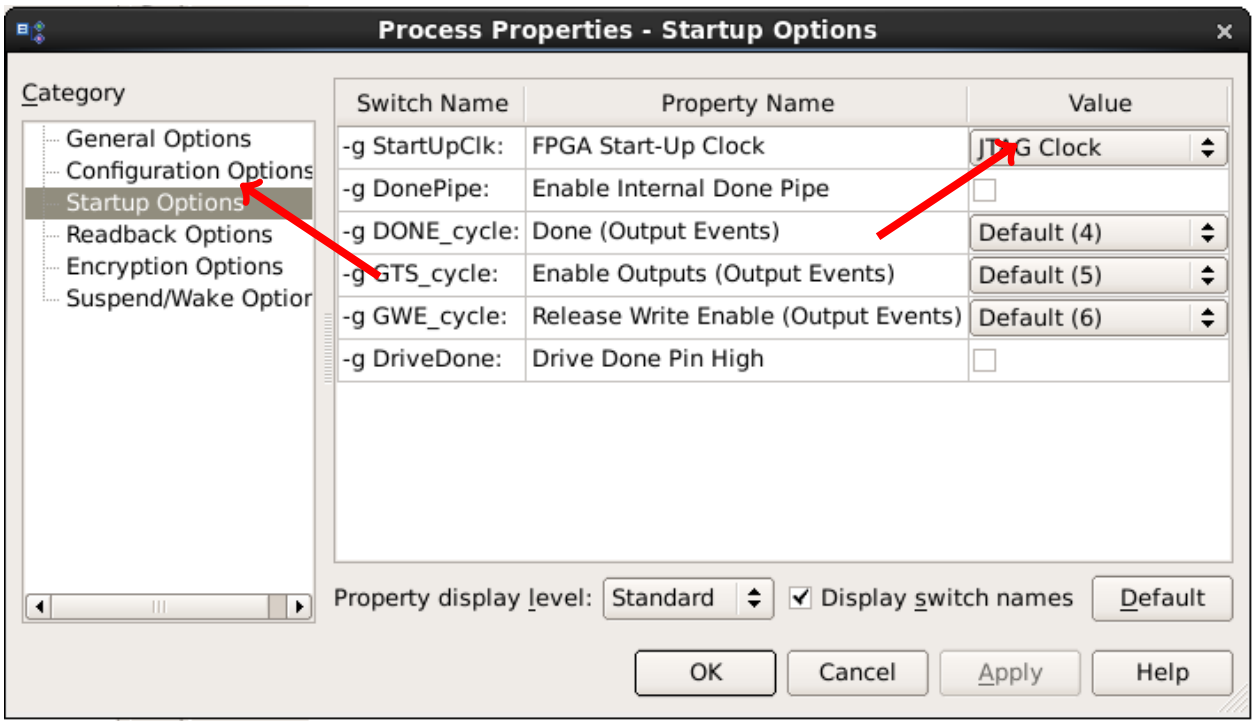

Figure 22: Setting the startup clock in the Process Properties window.

Choose the Startup Options category and set the switch name -g StartUpClk value to **JTAG clock**. Press **Apply** then **OK**.

4. Finally, left double-click Generate Programming File to generate the programming file (the "bitstream") that will be downloaded to the FPGA.

   It is possible to go straight to generating the programming file, and the Project Navigator will determine which of the previous steps need to be run to produce an up to date programming file.

5. When the generation of the bit-stream stage has completed successfully you will see the following message on the console panel:
   `Process "Generate Programming File" completed successfully`

9 Downloading the design to the FPGA

Downloading a bit-stream to the FPGA is accomplished via the Digilent **Adept** tool for NEXYS 3 board.

To download the design using the Digilent **Adept** tool:

1. Connect the NEXYS 3 Board to the computer: plug the micro USB cable into the **USB PROG** connector on the board, and connect the other end of the cable into the computer.
2. Turn on the NEXYS 3 Board using the toggle switch beside the USB connector.
3. Load the Digilent Adept tool from the Start Menu: → **Digilent** → **Adept**

   The Digilent Adept window will appear as seen in Figure 23.

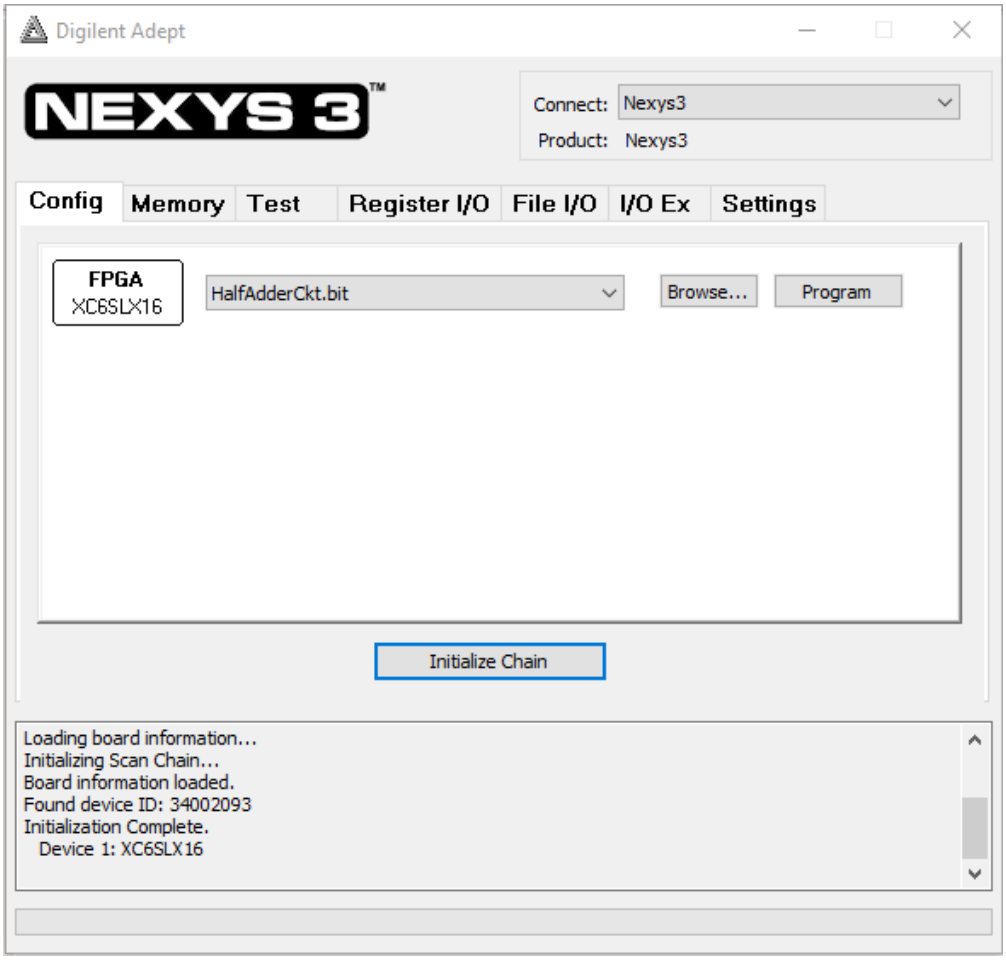

Figure 23: Digilent Adept FPGA programming tool.

4. Ensure that **Nexys 3** is selected under the Connect drop-down menu. If the Nexys 3 option does not appear, ensure the board is plugged in and turned on.

5. Select the Config tab if it is not already selected.

6. Click the **Browse** icon. A new window will appear to choose your bit file.

7. Navigate to the directory where your bit file resides (C:\XilinxShare\SchemCapHalfAdder) and double-click the HalfAdderCkt.bit file.

8. Click the **Program** button. The system will start to program the device and at the bottom of the Adept Tool you will see some messages indicating that it has successfully programmed the device. On the board, the yellow DONE light should glow.

10 Testing the Design

Depending on the state of the inputs, you may or may not see some of the LEDs on the bar-graph display glowing. We have assigned:

1. The Sum bit (S) to **LEDs** LD_0.

2. The carry bit (C) is displayed on **LED** LD_1.

We are using the slide switches for our A and B inputs.

1. The A inputs is assigned to **Switch** SW_1.

2. The B input is assigned to **Switch** SW_0.

Moving a switch to the **ON** position puts a 1 on the input. Moving a switch to the **OFF** position puts a 0 on the input.
Try different combinations of inputs and verify that the circuit is working correctly.

11 Appendix A - Setting-up and Testing the NEXYS3 board

This is intended to allow the student to quickly set up the NEXYS 3 board for this tutorial. It does not attempt to explain the configuration and is in no way a substitute for the documentation provided with the board. It will allow you to use the slide switches as input and the LEDs as outputs.

1. Connect the USB cable to the NEXYS 3 board.
2. Connect the host computer to your USB cable.
3. When the power switch to the board is on a small yellow LED labeled *Done* should glow.

You can test if the Digilent NEXYS3 Board is operational by using the Digilent Adept Tool. First, open the Adept Tool from the . Press the **Test** icon. A new menu will appear. Press Start Peripherals Test.

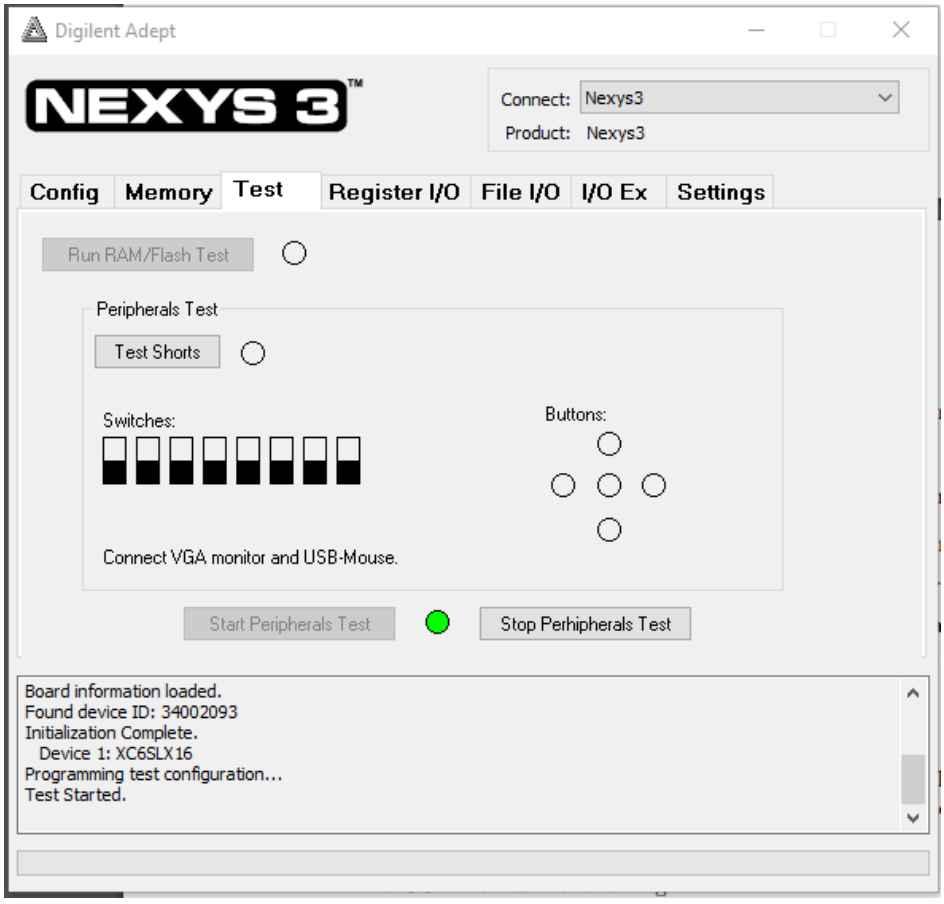

Figure 24: Peripheral test screen.

The test will display different values on the 7-segment display. You can also test the switches and light emitting diodes by sliding the switches to the on-off position. Once a switch is turned on the corresponding LED will glow. You will also notice that the switches on the Digilent Adept tool will change value. You can also test the push buttons by pressing on them. You will see the color of the corresponding button on the Adept tool change from transparent to black.

Once you are satisfied that the FPGA board is operational you can press the "Stop Peripherals Test". By pressing the "Reset Button" on the FPGA you will reset the board to the factory setting where it tests all other modules on the PCB board. Power off the board using the slide switch found at the top left part of the board.

12 Appendix B - LEDs, 7-Segments and Switches

The following sections explain the connection and location of the toggle switches and LEDs of the Digilent NEXYS 3 Board.

12.1 LEDs

The Digilent NEXYS 3 Board provides a series of eight LEDs (LD0–LD7) for use. All of these LEDs are **Logic Active High** meaning that an LED segment will glow when a logic high is applied to it. Table 1 shows the connection from the NEXYS 3 Board to LEDs expressed as UCF constraints.

—Description	—Location
NET LD0	LOC=U16
NET LD1	LOC=V16
NET LD2	LOC=U15
NET LD3	LOC=V15
NET LD4	LOC=M11
NET LD5	LOC=N11
NET LD6	LOC=R11
NET LD7	LOC=T11

Table 1: NEXYS 3 LED pin locations.

12.2 Seven Segment Displays

The Digilent NEXYS 3 Board provides four multiplexed 7-segment displays for use. The following tables show the connection from the NEXYS 3 Board to the 7-segment displays expressed as UCF constraints.

—Description	—Location
NET CA	LOC=T17;
NET CB	LOC=T18;
NET CC	LOC=U17;
NET CD	LOC=U18;
NET CE	LOC=M14;
NET CF	LOC=N14;
NET CG	LOC=L14;
NET DP	LOC=M13;
NET AN0	LOC=N16;
NET AN1	LOC=N15;
NET AN2	LOC=P19;
NET AN3	LOC=P17

Table 2: NEXYS 3 seven segment display pin locations.

12.3 Slide Switches

The Digilent NEXYS 3 board has a bank of eight toggle switches which are accessible by the user. When closed or ON, each toggle switch pulls the connected pin of the NEXYS 3 Board to ground. When the toggle switch is open or OFF, the pin is pulled high through a $10K\Omega$ resistor.

The table below shows the connections from the Digilent NEXYS 3 Board to the switches expressed as UCF constraints.

—Description	—Location
NET SW0	LOC=T10
NET SW1	LOC=T9
NET SW2	LOC=V9
NET SW3	LOC=M8
NET SW4	LOC=N8
NET SW5	LOC=U8
NET SW6	LOC=V8
NET SW7	LOC=T5

Table 3: NEXYS 3 slide switch pin locations.

12.4 Push Buttons

The Digilent NEXYS 3 board has five pushbuttons (labeled BTNS through BTNR) which are accessible by the user.

When pressed, each pushbutton pulls the connected pin of the NEXYS 3 Board to ground. Otherwise, the pin is pulled high through a $10K\Omega$ resistor. The table below shows the connections

from the the Digilent NEXYS 3 Board to the push buttons expressed as UCF constraints.

—Description	—Location
NET BTNS	LOC=B8
NET BTNU	LOC=A8
NET BTNL	LOC=C4
NET BTND	LOC=C9
NET BTNR	LOC=D9

Table 4: NEXYS 3 pushbutton pin locations.